Table 1 shows all pins for the EP1M120 484-pin FineLine BGA package.

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
1		I/O	HSDI_RX1p	A16
1		I/O	HSDI_RX2p	A15
1		I/O	HSDI_RX3p	A14
1		I/O	HSDI_RX4p	A13
1		HSDI_CLK1p	-	B12
1		I/O	VREF1 (3)	A17
1		I/O	HSDI_RX1n	B16
1		I/O	HSDI_RX2n	B15
1		I/O	HSDI_RX3n	B14
1		I/O	HSDI_RX4n	B13
1		HSDI_CLK1n	-	A12
2 (4)		I/O	HSDI_TX1p	AB16
2 (4)		I/O	HSDI_TX2p	AB15
2 (4)		I/O	HSDI_TX3p	AB14
2 (4)		I/O	HSDI_TX4p	AB13
2 (4)		HSDI_TXCLKOUT1p	-	AB12
2 (4)		I/O	VREF2 (3)	AB17
2 (4)		I/O	HSDI_TX1n	AA16
2 (4)		I/O	HSDI_TX2n	AA15
2 (4)		I/O	HSDI_TX3n	AA14
2 (4)		I/O	HSDI_TX4n	AA13
2 (4)		HSDI_TXCLKOUT1n	-	AA12
3		HSDI_CLK2p	-	A11
3		I/O	HSDI_RX5p	A10
3		I/O	HSDI_RX6p	A9
3		I/O	HSDI_RX7p	A8
3		I/O	HSDI_RX8p	A7
3		HSDI_CLK2n	-	B11
3		I/O	VREF3 (3)	C10
3		I/O	HSDI_RX5n	B10
3		I/O	HSDI_RX6n	B9
3		I/O	HSDI_RX7n	B8
3		I/O	HSDI_RX8n	B7
4 (4)		I/O	HSDI_TX5p	AB10
4 (4)		I/O	HSDI_TX6p	AB9
4 (4)		I/O	HSDI_TX7p	AB8
4 (4)		I/O	HSDI_TX8p	AB7
4 (4)		I/O	VREF4 (3)	AB11
4 (4)		I/O	HSDI_TX5n	AA10
4 (4)		I/O	HSDI_TX6n	AA9
4 (4)		I/O	HSDI_TX7n	AA8
4 (4)		I/O	HSDI_TX8n	AA7
5	A	I/O	-	B19
5	A	I/O	-	C19
5	A	I/O	-	D18
5	A	I/O	-	C17
5	A	I/O	-	D19
5	A	I/O	-	D17
5	A	I/O	-	B18
5	A	I/O	-	C18
5	A	I/O	-	E14
5	A	I/O	-	E18
5	A	I/O	-	F15
5	A	I/O	VREF5 (3)	F18
5	A	I/O	-	B17
5	A	I/O	-	C16
5	B	I/O	-	D16

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
5	B	I/O	-	E13
5	B	I/O	-	F13
5	B	I/O	-	E15
5	C	I/O	FAST_ROW2 (5)	H12
6	A	I/O	FAST_ROW1 (5)	H11
6	B	I/O	-	C3
6	B	I/O	-	A5
6	B	I/O	-	B4
6	B	I/O	-	C4
6	B	I/O	-	B3
6	C	I/O	-	D6
6	C	I/O	-	E8
6	C	I/O	-	B5
6	C	I/O	-	D7
6	C	I/O	-	C5
6	C	I/O	-	E10
6	C	I/O	-	D5
6	C	I/O	-	A6
6	C	I/O	-	A3
6	C	I/O	-	A4
6	C	I/O	VREF6 (3)	D4
7	A	I/O	DATA1 (6)	J22
7	A	I/O	DATA2 (6)	J21
7	A	I/O	DATA3 (6)	J20
7	A	I/O	INIT_DONE (7)	H19
7	A	I/O	DATA4 (6)	K21
7	A	I/O	nWS (6)	J19
7	A	I/O	-	K22
7	A	I/O	DATA5 (6)	K20
7	A	I/O	nCS (6)	J18
7	A	I/O	DATA7 (6)	L21
7	A	I/O	nRS (6)	K19
7	A	I/O	VREF7 (3)	L22
7	A	I/O	DATA6 (6)	L20
7	A	I/O	CLKUSR (6)	L19
7	A	I/O	CS (6)	L18
7	B	I/O	DEV_CLRn (7)	H18
7	B	I/O	DEV_OE (7)	H17
7	B	I/O	-	F20
7	B	I/O	-	F21
7	B	I/O	-	H21
7	B	I/O	-	F22
7	B	I/O	-	H15
7	B	I/O	RDYnBSY (6)	K18
7	B	I/O	-	G20
7	B	I/O	-	G21
7	B	I/O	-	M21
7	B	I/O	-	M20
7	C	I/O	-	E19
7	C	I/O	-	K15
7	C	I/O	FAST6 (8)	L14
7	C	I/O	-	F19
7	C	I/O	-	H13
7	C	I/O	-	J17
7	C	I/O	FAST4 (8)	K13
7	C	I/O	-	L17
7	C	I/O	-	L15
7	C	I/O	FAST_ROW4 (5)	K12
7	C	I/O	-	M19

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
7	C	I/O	-	L16
7	C	I/O	FAST5 (8)	K14
8	A	I/O	FAST3 (8)	L9
8	A	I/O	-	H1
8	A	I/O	-	J2
8	A	I/O	-	K3
8	A	I/O	FAST2 (8)	K9
8	A	I/O	-	G2
8	A	I/O	FAST1 (8)	K10
8	A	I/O	-	J1
8	A	I/O	-	F2
8	A	I/O	-	L2
8	A	I/O	-	H2
8	A	I/O	FAST_ROW3 (5)	K11
8	A	I/O	-	K1
8	A	I/O	-	K2
8	A	I/O	-	L3
8	B	I/O	-	G3
8	B	I/O	-	H4
8	B	I/O	-	E5
8	B	I/O	-	K4
8	B	I/O	-	G11
8	B	I/O	-	H3
8	B	I/O	-	J5
8	B	I/O	-	J3
8	B	I/O	-	L5
8	B	I/O	-	L4
8	B	I/O	-	J4
8	B	I/O	-	K5
8	C	I/O	-	E9
8	C	I/O	LOCK1 (9)	F3
8	C	I/O	-	J8
8	C	I/O	-	F9
8	C	I/O	-	F5
8	C	I/O	-	H7
8	C	I/O	-	J6
8	C	I/O	-	J10
8	C	I/O	-	K8
8	C	I/O	-	H5
8	C	I/O	-	H6
8	C	I/O	VREF8 (3)	L1
9	A	I/O	-	N22
9	A	I/O	-	N20
9	A	I/O	-	R20
9	A	I/O	-	N18
9	A	I/O	-	N21
9	A	I/O	-	N19
9	A	I/O	-	M22
9	A	I/O	-	R21
9	A	I/O	-	P19
9	A	I/O	-	U22
9	A	I/O	-	P20
9	A	I/O	VREF9 (3)	P21
9	A	I/O	-	T22
9	A	I/O	-	T21
9	A	I/O	-	T20
9	B	I/O	-	N17
9	B	I/O	-	M16
9	B	I/O	-	T12

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
9	B	I/O	-	P17
9	B	I/O	-	M15
9	B	I/O	-	P18
9	B	I/O	-	N15
9	B	I/O	-	R19
9	B	I/O	-	N16
9	B	I/O	-	T19
9	B	I/O	-	R14
9	B	I/O	-	R15
9	C	I/O	-	R12
9	C	I/O	-	P12
9	C	I/O	-	N13
9	C	I/O	-	T13
9	C	I/O	-	M14
9	C	I/O	-	R13
9	C	I/O	FAST_ROW6 (5)	N12
9	C	I/O	-	N14
9	C	I/O	-	P13
10	A	I/O	-	U1
10	A	I/O	-	M1
10	A	I/O	-	N2
10	A	I/O	-	U2
10	A	I/O	-	T1
10	A	I/O	-	M2
10	A	I/O	-	N1
10	A	I/O	-	R2
10	A	I/O	FAST_ROW5 (5)	N11
10	A	I/O	-	T2
10	A	I/O	-	T3
10	B	I/O	-	P3
10	B	I/O	-	R4
10	B	I/O	-	M4
10	B	I/O	-	M3
10	B	I/O	-	N4
10	B	I/O	-	N3
10	B	I/O	-	P5
10	B	I/O	-	R3
10	B	I/O	-	R5
10	B	I/O	-	T4
10	B	I/O	-	P4
10	B	I/O	-	N9
10	C	I/O	-	L6
10	C	I/O	-	L7
10	C	I/O	-	L8
10	C	I/O	-	M5
10	C	I/O	-	M8
10	C	I/O	-	P6
10	C	I/O	-	M9
10	C	I/O	LOCK2 (9)	U3
10	C	I/O	-	P10
10	C	I/O	-	P11
10	C	I/O	-	N8
10	C	I/O	-	N10
10	C	I/O	VREF10 (3)	P2
11	A	I/O	VREF11 (3)	U20
11	A	I/O	-	AA20
11	A	I/O	-	U14
11	A	I/O	-	Y18
11	A	I/O	-	Y20

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
11	A	I/O	-	AB19
11	A	I/O	-	V21
11	A	I/O	-	W20
11	A	I/O	-	AA19
11	A	I/O	-	V20
11	A	I/O	-	U19
11	A	I/O	-	Y19
11	A	I/O	-	U21
11	A	I/O	-	W21
11	A	I/O	-	Y21
11	B	I/O	-	U15
11	B	I/O	-	W16
11	B	I/O	-	AA11
11	B	I/O	-	AB18
11	B	I/O	-	T15
11	B	I/O	-	W18
11	B	I/O	-	AA17
11	B	I/O	-	Y17
11	B	I/O	-	V19
11	B	I/O	-	W19
11	B	I/O	-	AA18
11	B	I/O	-	W17
11	C	I/O	-	Y11
11	C	I/O	-	W11
11	C	I/O	-	Y12
11	C	I/O	-	Y14
11	C	I/O	-	W12
11	C	I/O	-	W14
11	C	I/O	-	V12
11	C	I/O	-	Y15
11	C	I/O	-	Y13
11	C	I/O	FAST_ROW8 (5)	U12
11	C	I/O	-	Y16
11	C	I/O	-	W15
11	C	I/O	-	W13
12	A	I/O	-	AB3
12	A	I/O	-	Y3
12	A	I/O	-	Y4
12	A	I/O	-	AA5
12	A	I/O	-	AA3
12	A	I/O	-	Y5
12	A	I/O	FAST_ROW7 (5)	U11
12	A	I/O	-	AA4
12	A	I/O	-	W5
12	A	I/O	-	W4
12	A	I/O	-	AB6
12	A	I/O	-	AB4
12	A	I/O	-	AB5
12	A	I/O	-	AA6
12	A	I/O	-	Y7
12	B	I/O	-	V5
12	B	I/O	-	R6
12	B	I/O	-	R7
12	B	I/O	-	U8
12	B	I/O	-	Y8
12	B	I/O	-	Y6
12	B	I/O	-	V8
12	B	I/O	-	W6
12	B	I/O	-	Y9

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
12	B	I/O	-	W7
12	B	I/O	-	W9
12	B	I/O	-	V9
12	C	I/O	-	R8
12	C	I/O	VREF12 (3)	U9
12	C	I/O	-	W8
12	C	I/O	-	R9
12	C	I/O	-	Y10
12	C	I/O	-	U10
12	C	I/O	-	W10
12	C	I/O	-	R10
12	C	I/O	-	R11
13		DATA0 (10), (11)	-	D20
13		DCLK (10)	-	E21
13		CONF_DONE (10)	-	A22
13		nSTATUS (10)	-	A21
13		MSEL0 (10)	-	C21
13		MSEL1 (10)	-	E22
13		PLLRDY (10), (12)	-	E20
13		nCONFIG (10)	-	C20
13		nCE (10)	-	B21
13		VCCSEL (10), (13)	-	C22
13		nIO_PULLUP (10), (14)	-	D21
13		nCEO (10)	-	D22
13		CLKLK_ENA (10), (15)	-	B20
14		TDO (10)	-	Y22
14		TDI (10)	-	AA22
14		TMS (10)	-	AB22
14		TCK (10)	-	AB21
14		TRST (10)	-	AB20
15		CLKLK_OUT1p (10),	-	B1
15		CLKLK_OUT1n	-	C1
16		CLKLK_OUT2n	-	Y1
16		CLKLK_OUT2p (10),	-	AA1
10		CLKLK_FB1n	CLKLK_FB1VREF	E1
10		CLKLK_FB1p (10), (17)	-	D1
10		CLK1p	-	L10
10		CLK2p	-	L11
10		CLK1n	CLK1VREF	M10
10		CLK2n	CLK2VREF	M11
10		CLKLK_FB2n	CLKLK_FB2VREF	V1
10		CLKLK_FB2p (17)	-	W1
9		CLK3p	-	L12
9		CLK4p	-	L13
9		CLK3n	CLK3VREF	M12
9		CLK4n	CLK4VREF	M13
-		RES0 (18)	-	D11
-		VCCINT	-	G19
-		VCCINT	-	M18
-		VCCINT	-	T18
-		VCCINT	-	V18
-		VCCINT	-	G17
-		VCCINT	-	K17
-		VCCINT	-	G16
-		VCCINT	-	T16
-		VCCINT	-	V16
-		VCCINT	-	J16
-		VCCINT	-	T7
-		VCCINT	-	V6

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
-		VCCINT	-	J7
-		VCCINT	-	K7
-		VCCINT	-	M7
-		VCCINT	-	V7
-		VCCINT	-	G9
-		VCCINT	-	T6
-		VCCINT	-	F11
-		VCCIO1	-	F16
-		VCCIO3	-	F7
-		VCCIO4	-	G7
-		VCCIO4	-	D12
-		VCCIO4	-	G18
-		VCCIO5	-	F17
-		VCCIO5	-	A19
-		VCCIO6	-	F6
-		VCCIO6	-	A2
-		VCCIO7	-	G22
-		VCCIO7	-	H16
-		VCCIO7	-	H20
-		VCCIO7	-	H22
-		VCCIO8	-	G6
-		VCCIO8	-	G5
-		VCCIO8	-	G4
-		VCCIO8	-	F1
-		VCCIO9	-	P22
-		VCCIO9	-	R16
-		VCCIO9	-	R17
-		VCCIO9	-	R18
-		VCCIO10	-	N5
-		VCCIO10	-	N6
-		VCCIO10	-	N7
-		VCCIO10	-	P1
-		VCCIO11	-	V22
-		VCCIO11	-	U16
-		VCCIO11	-	U17
-		VCCIO11	-	U18
-		VCCIO12	-	U5
-		VCCIO12	-	U6
-		VCCIO12	-	U7
-		VCCIO12	-	AB1
-		VCCIO13	-	A20
-		VCCIO14	-	AA21
-		VCCD_RX	-	E16
-		VCCD_RX	-	E7
-		VCCD_RX	-	G10
-		VCCD_RX	-	G13
-		VCCD_RX	-	J11
-		VCCD_TX	-	E17
-		VCCD_TX	-	E6
-		VCCA_HSDI1	-	F10
-		VCCD_HSDI1	-	E11
-		VCCA_HSDI2	-	E12
-		VCCD_HSDI2	-	F12
-		VCCA_CKLK1	-	B2
-		VCCA_CKLK1	-	D2
-		VCCD_CKLK1	-	E2
-		VCCA_CKLK2	-	AA2
-		VCCA_CKLK2	-	W2
-		VCCD_CKLK2	-	V2

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
		VCC_CKOUT1	-	C2
		VCC_CKOUT2	-	Y2
-		GND	-	H14
-		GND	-	R22
-		GND	-	W22
-		GND	-	A18
-		GND	-	G12
-		GND	-	M17
-		GND	-	T17
-		GND	-	V17
-		GND	-	G15
-		GND	-	J13
-		GND	-	K16
-		GND	-	P16
-		GND	-	V15
-		GND	-	C15
-		GND	-	D15
-		GND	-	J15
-		GND	-	P15
-		GND	-	C14
-		GND	-	D14
-		GND	-	F14
-		GND	-	G14
-		GND	-	J14
-		GND	-	P14
-		GND	-	T14
-		GND	-	V14
-		GND	-	C13
-		GND	-	U13
-		GND	-	V13
-		GND	-	C12
-		GND	-	J12
-		GND	-	H10
-		GND	-	T10
-		GND	-	V10
-		GND	-	C9
-		GND	-	D9
-		GND	-	H9
-		GND	-	J9
-		GND	-	P9
-		GND	-	T9
-		GND	-	C8
-		GND	-	D8
-		GND	-	F8
-		GND	-	H8
-		GND	-	P8
-		GND	-	T8
-		GND	-	C7
-		GND	-	P7
-		GND	-	T11
-		GND	-	B6
-		GND	-	C6
-		GND	-	K6
-		GND	-	M6
-		GND	-	V11
-		GND	-	G8
-		GND	-	T5
-		GND	-	AB2
-		GND	-	A1

Table 1. EP1M120 Device Pin-Outs				
I/O and VREF Bank	**Maximum GTL+ Current Subgroup** (1)	**Pin Name/Function**	**Dual Purpose Function** (2)	**484-Pin FineLine BGA**
-		GND	-	G1
-		GND	-	R1
		GND		U4
		GND		V4
		GND		V3
		GND		D3
		GND		E4
		GND		E3
		GND		F4
		GND		W3
-		GND	-	D13
-		GND	-	D10
-		GND	-	C11
-		GND	-	B22
Total User I/O Pins (19)				303

Notes:

(1) For a given bank, there are I/O subgroups marked by letters A, B, C, or D. For example, in I/O Bank 11, there are 15 I/O pins in group A. For any power group A, B, C, or D, there is a maximum of 12 outputs that can use the GTL+ I/O standard when no other outputs reside in that

(2) If HSDI circuitry is used (e.g., source synchronous or CDR), then all unused I/O pins in Banks 1, 2, 3, and 4 cannot be used. The unused pins should be connected to GND on the board to help noise immunity.

(3) If a bank is used for a voltage-referenced I/O standard, then this pin is the voltage-reference pin for the bank. If a voltage-referenced standard is not used, then this pin is a user I/O pin.

(4) Banks 2 and 4 must have the same VCCIO level, but can have different VREF levels.

(5) This pin is a dual-purpose pin used for driving the row global signals within an I/O bank's associated LAB row. If this pin is not used to drive global row signals, it can be used as a user I/O pin. Banks 2 and 4 share the same power supply; therefore, power pins for only bank 4 will

(6) This pin can be used as a user I/O pin after configuration.

(7) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration

(8) This pin is a dual-purpose pin used for driving the dedicated global fast lines within the entire device. If this pin is not used to drive global fast lines, it is a user I/O pin.

(9) This pin shows the status of the general purpose PLL. When the general purpose PLL is locked to the incoming clock, LOCK drives high. LOCK remains high if a periodic clock remains clocking. If the LOCK function is not used, this pin is a user I/O pin.

(10) This pin is a dedicated pin; it is not available as a user I/O pin.

(11) This pin is tri-stated in user mode.

(12) Dedicated output that shows the LOCK status of all PLLs. This signal is the AND gate of all PLL LOCK signals (for all enabled HSDI PLLs and GPLLs) and CONF_DONE. This pin should be unconnected if its function is not used.

(13) This pin is a dedicated input that is used to choose whether programming input pins (dedicated configuration and JTAG pins) can accept 3.3 V/2.5 V or 1.8 V during configuration. A logic high sets 3.3 V/2.5 V, and a logic low sets 1.8 V. V_{IH} and VIL are determined by VCCIO13 voltage settings. This pin's input voltage is determined by VCCIO13. If VCCIO13 is 3.3 V, a logic high is determined by a 3.3-V LVTTL V_{IH} minimum. If VCCIO13 is 2.5 V, a logic high is determined by a 2.5-V LVTTL V_{IH} minimum. If VCCIO13 is 1.8 V, a logic high is deternined by a 1.8-V LVTTL V_{IH}

(14) This pin is a dedicated input that is used to control whether weak active pull-up resistors are on for all I/O pins during power-up and configuration. A logic low means that active pull-up resistors are enabled, and a logic high means that active pull-up resistors are disabled. VIH and VIL are determined by VCCIO13 voltage settings. This pin's input voltage is determined by VCCIO13. If VCCIO13 is 3.3 V, a logic high is determined by a 3.3-V LVTTL V_{IH} minimum. If VCCIO13 is 2.5 V, a logic high is determined by a 2.5-V LVTTL V_{IH} minimum. If VCCIO13 is 1.8 V, a logic high is determined by a 1.8-V LVTTL V_{IH} minimum.

(15) This pin is a dedicated input that is the active high enable pin for all the general purpose PLL circuits in the device. When deasserted, all general purpose PLLs are reset to their default unlocked state and will stop clocking. Once reasserted, the PLLs will lock again and start clocking. This PLL enable control can be selected for each general purpose PLL. If this pin feature is not used, connect the pin to GND on the board, and the pin is a floating input.

(16) This pin is a dedicated external clock output from a general purpose PLL. CLKLK_OUT1p is from general purpose PLL1, and CLKLK_OUT2p is from general purpose PLL2. Each dedicated clock output has its own VCCIO power for the output standard selection. If this pin feature is not used, it should be connected to GND on the board.

(17) This pin is a dedicated external clock feedback for a general purpose PLL. CLKLK_FB1p feeds general purpose PLL1, and CLKLK_FB2p feeds general purpose PLL2. The external clock feedback must use the same I/O standard as the external clock output and the global clock input to the general purpose PLL. If this pin feature is not used, connect this pin to GND on the board.

(18) This pin has no device function and can be connected straight to GND.

(19) The user I/O pin count includes dedicated clock inputs and HSDI pins.

Table 2 shows the output pin placement guideline with respect to VREF pins. Output pins should be placed two balls away from a VREF pin that is used within a bank. Table 2 shows which pins cannot be used as outputs because they are neighbors to the specified VREF pin. These pins can still be used as inputs. If a VREF pin is being used as a regular I/O, this output pin placement guideline does not apply to that pin.

Table 2. Output Pin-to-VREF Pin Placement Guidelines

VREF Pin	Adjacent Pins That Cannot Be Outputs
VREF1	A16
	B16
VREF2	AB16
	AA16
VREF3	A10
	B10
VREF4	AB10
	AA10
VREF5	B18
	E18
	B19
	D19
	C18
VREF6	D5
	E10
	A6
VREF7	K22
	L21
	J22
	K21
	K20
VREF8	J6
	K8
	H7
	J10
	J8
VREF9	M22
	U22
	N22
	N21
	R21
VREF10	U3
	P11
	M9
	P10
	L8
VREF11	Y20
	W20
	U21
	V21
	V20
VREF12	R9
	R11
	W10
	Y10
	R10

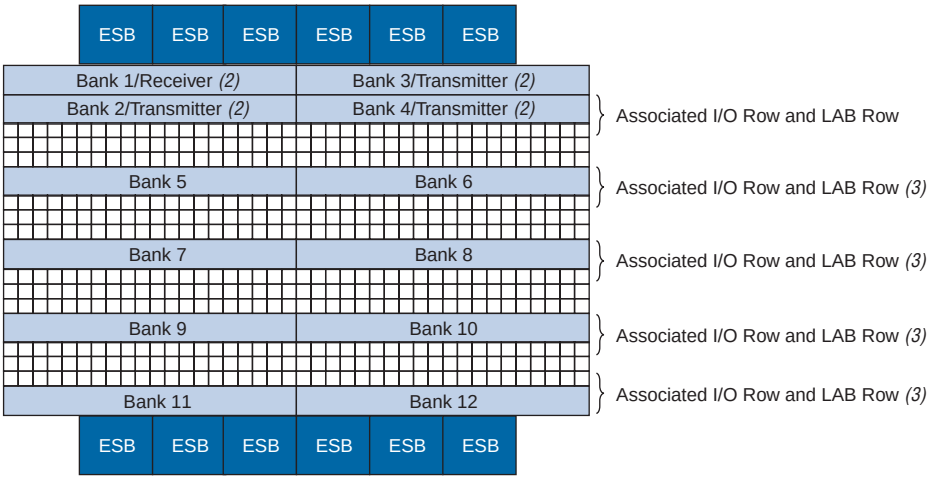
Table 3 provides descriptions for all power, HSDI, and general-purpose phase-locked loop (PLL) related pins.

Table 3. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
HSDI_CLK1p	Dedicated input pin that drives HSDI PLL1 for high speed differential interface.
HSDI_CLK1n	Dedicated negative terminal input for differential clock into HSDI PLL1.
HSDI_CLK2p	Dedicated input pin that drives HSDI PLL2 for high speed differential interface.
HSDI_CLK2n	Dedicated negative terminal input for differential clock into HSDI PLL2.
HSDI_TXCLKOUT1p	Dedicated output pin for source synchronous transmission from HSDI.
HSDI_TXCLKOUT1n	Dedicated negative terminal output for differential source synchronous clock from HSDI.
HSDI_RX[1..8]p/n	Dual-purpose pins for HSDI receiver channels 1 through 8; "p" is positive terminal, "n" is negative terminal. These pins can only be used as regular I/O pins if HSDI circuitry is not
HSDI_TX[1..8]p/n	Dual-purpose pins for HSDI transmitter channels 1 through 8; "p" is positive terminal, "n" is negative terminal. These pins can only be used as regular I/O pins if HSDI circuitry is not
VREF[1..12]	VREF pins for each I/O bank; VREF1 is the reference voltage pin for BANK1, VREF2 for BANK2, VREF3 for BANK3, etc. These pins are regular I/O pins if the I/O Bank is not using a VREF I/O standard.
FAST_ROW[1..8]	Dual-purpose pins for driving the row global signals within an I/O bank are associated with a LAB row. These pins are regular I/O pins if not used to drive row globals.
FAST[1..6]	Dual-purpose pins for driving the dedicated global fast lines within the entire device. These pins are regular I/O pins if not used to drive fast global signals.
CLK1p	Dedicated global clock input. Also, the clock input to general-purpose PLL 1.
CLK1n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK1VREF) for the CLK1p input.
CLK2p	Dedicated global clock input. Also, the clock input to general-purpose PLL 2.
CLK2n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK2VREF) for the CLK2p input.
CLK3p	Dedicated global clock input.
CLK3n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK3VREF) for the CLK3p input.
CLK4p	Dedicated global clock input.
CLK4n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK3VREF) for the CLK3p input.
CLKLK_OUT1p	Dedicated external output for general-purpose PLL 1.
CLKLK_OUT1n	Dedicated negative terminal output for differential output from general-purpose PLL 1.
CLKLK_OUT2p	Dedicated external output for general-purpose PLL 2.
CLKLK_OUT2n	Dedicated negative terminal output for differential output from general-purpose PLL 2.
CLKLK_FBIN1p	Dedicated clock input for the external feedback to general-purpose PLL 1.
CLKLK_FBIN1n	Dedicated negative terminal input for differential external feedback from general-purpose PLL 1. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLKLK_FBIN1VREF) for the clock feedback input.
CLKLK_FBIN2p	Dedicated clock input for the external feedback to general-purpose PLL 2.
CLKLK_FBIN2n	Dedicated negative terminal input for differential external feedback from general-purpose PLL 2. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLKLK_FBIN2VREF) for the clock feedback input.
PLLRDY	Dedicated output that shows the lock status of all PLLs. This signal is the AND gate of all PLL Lock signals (HSDI PLL and general-purpose PLL) and CONF_DONE. If used, this pin should be left unconnected.
VCCSEL	Dedicated input that is used to choose whether programming input pins (dedicated configuration and JTAG pins) can accept 3.3 V, 2.5 V, or 1.8 V during configuration. A "1" means 3.3 V or 2.5 V, and a "0" means 1.8 V.

Pin Name	Pin Description
nIO_PULLUP	Dedicated input that is used to control whether weak active pull-up resistors are on for all I/O pins during power-up and configuration. A "0" means active pull-up resistors are enabled; a "1" means that they are disabled.
RES0	This pin has no device function and can be connected straight to GND.
VCCINT	Internal core voltage. This must be 1.8 V.
VCCIO[1..14]	I/O and configuration pin voltage. For I/O banks these can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V. For configuration and JTAG banks, these can be 3.3 V, 2.5 V, or 1.8 V.
VCCD_RX	Digital power for HSDI receivers. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCD_TX	Digital power for HSDI transmitters. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_HSDI1	Analog power for HSDI PLL 1. These must be connected to 1.8 V. HSDI 1 and 2 analog power should be isolated with its own partition in the VCCINT plane.
VCCD_HSDI1	Digital power for HSDI PLL 1. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_HSDI2	Analog power for HSDI PLL 2. These must be connected to 1.8 V. HSDI 1 and 2 analog power should be isolated with its own partition in the VCCINT plane.
VCCD_HSDI2	Digital power for HSDI PLL 2. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_CKLK1	Analog power for general-purpose PLL 1. These must be connected to 1.8 V. General-purpose PLL 1 and 2 analog power should be isolated with its own partition in the VCCINT
VCCD_CKLK1	Digital power for general-purpose PLL 1. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_CKLK2	Analog power for general-purpose PLL 2. These must be connected to 1.8 V. General-purpose PLL 1 and 2 analog power should be isolated with its own partition in the VCCINT
VCCD_CKLK2	Digital power for general-purpose PLL 2. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCC_CKOUT1	External clock output buffer power for CLKLK_OUT1p/n of general-purpose PLL 1. This can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
VCC_CKOUT2	External clock output buffer power for CLKLK_OUT2p/n of general-purpose PLL 2. This can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.

Figure 1 shows the I/O and HSDI bank block diagram for the EP1M120 device.

Figure 1. I/O & HSDI Banks *Note (1)*



Notes:
(1) The following banks are not shown: Bank 13 (contains dedicated configuration and control pins), Bank 14 (contains dedicated JTAG pins: `TCK`, `TDI`, `TDO`, `TMS`, and `TRST`), Bank 15 (contains `CLKLK_OUT1p/n` and its output power), Bank 16 (contains `CLKLK_OUT2p/n` and its output power).
(2) The top I/O banks 1, 2, 3, and 4 only support non-HSDI I/O pins when the HSDI circuitry is unused. If any HSDI channel is used, banks 1, 2, 3, and 4 do not support regular I/O pins.
(3) `fast_row` pins feed the row global signals in the LAB row associated with the I/O bank. For I/O banks 1 through 10, these banks are associated with the LAB row directly below them. Banks 11 and 12 are associated with the LAB row directly above them. I/O banks 1 through 4 do not have `fast_row` pins.