Pin Information For The Stratix™ EP1S80 Device, ver 2.0

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT			VCC	VCC			
		VCCA_PLL7			L23	J31			
		GND			GND	GND			
		GNDA_PLL7			M23	K31			
		VCCG_PLL7			J23	L30			
		GNDG_PLL7			K23	L31			
B2	VREF0B2	FPLL7CLKp			E31	J38			
B2	VREF0B2	FPLL7CLKn			D31	J39			
B2	VREF0B2	IO				P26			
B2	VREF0B2	IO				R26			
B2	VREF0B2	IO	DIFFIO_RX75p			F34			LOW
B2	VREF0B2	IO	DIFFIO_RX75n			F35			LOW
B2	VREF0B2	IO	DIFFIO_TX75p			T26			LOW
B2	VREF0B2	IO	DIFFIO_TX75n			U26			LOW
B2	VREF0B2	IO	DIFFIO_RX74p			H35			LOW
B2	VREF0B2	IO	DIFFIO_RX74n			H34			LOW
B2	VREF0B2	IO	DIFFIO_TX74p			U27			LOW
B2	VREF0B2	IO	DIFFIO_TX74n			T27			LOW
B2	VREF0B2	IO	DIFFIO_RX73p			G35			LOW
B2	VREF0B2	IO	DIFFIO_RX73n			G34			LOW
B2	VREF0B2	IO	DIFFIO_TX73p			P27			LOW
B2	VREF0B2	IO	DIFFIO_TX73n			R27			LOW
B2	VREF0B2	IO	DIFFIO_RX72p			J34			LOW
B2	VREF0B2	IO	DIFFIO_RX72n			J35			LOW
B2	VREF0B2	IO	DIFFIO_TX72p			T28			LOW
B2	VREF0B2	IO	DIFFIO_TX72n			T29			LOW
B2	VREF0B2	VREF0B2			L22	M29			
B2	VREF0B2	IO	DIFFIO_RX71p			D37			LOW
B2	VREF0B2	IO	DIFFIO_RX71n			C38			LOW
B2	VREF0B2	IO	DIFFIO_TX71p			P28			LOW
B2	VREF0B2	IO	DIFFIO_TX71n			R28			LOW
B2	VREF0B2	IO	DIFFIO_RX70p			F36			LOW
B2	VREF0B2	IO	DIFFIO_RX70n			F37			LOW
B2	VREF0B2	IO	DIFFIO_TX70p			N30			LOW
B2	VREF0B2	IO	DIFFIO_TX70n			N31			LOW
B2	VREF0B2	IO	DIFFIO_RX69p			G36			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF0B2	IO	DIFFIO_RX69n			G37			LOW
B2	VREF0B2	IO	DIFFIO_TX69p			P31			LOW
B2	VREF0B2	IO	DIFFIO_TX69n			P30			LOW
B2	VREF0B2	IO	DIFFIO_RX68p			H37			LOW
B2	VREF0B2	IO	DIFFIO_RX68n			H36			LOW
B2	VREF0B2	IO	DIFFIO_TX68p			R31			LOW
B2	VREF0B2	IO	DIFFIO_TX68n			R30			LOW
B2	VREF0B2	IO	DIFFIO_RX67p			D39			LOW
B2	VREF0B2	IO	DIFFIO_RX67n			D38			LOW
B2	VREF0B2	IO	DIFFIO_TX67p		K24	M30			LOW
B2	VREF0B2	IO	DIFFIO_TX67n		J24	M31			LOW
B2	VREF1B2	IO	DIFFIO_RX66p			E36			LOW
B2	VREF1B2	IO	DIFFIO_RX66n			E37			LOW
B2	VREF1B2	IO	DIFFIO_TX66p		K25	J32			LOW
B2	VREF1B2	IO	DIFFIO_TX66n		J25	J33			LOW
B2	VREF1B2	IO	DIFFIO_RX65p			E38			LOW
B2	VREF1B2	IO	DIFFIO_RX65n			E39			LOW
B2	VREF1B2	IO	DIFFIO_TX65p		H24	K32			LOW
B2	VREF1B2	IO	DIFFIO_TX65n		G24	K33			LOW
B2	VREF1B2	IO	DIFFIO_RX64p			F38			LOW
B2	VREF1B2	IO	DIFFIO_RX64n			F39			LOW
B2	VREF1B2	IO	DIFFIO_TX64p		H25	L33			LOW
B2	VREF1B2	IO	DIFFIO_TX64n		G25	L32			LOW
B2	VREF1B2	IO	DIFFIO_RX63p			G39			LOW
B2	VREF1B2	IO	DIFFIO_RX63n			G38			LOW
B2	VREF1B2	IO	DIFFIO_TX63p		K26	M32			LOW
B2	VREF1B2	IO	DIFFIO_TX63n		L26	M33			LOW
B2	VREF1B2	IO	DIFFIO_RX62p			H39			LOW
B2	VREF1B2	IO	DIFFIO_RX62n			H38			LOW
B2	VREF1B2	IO	DIFFIO_TX62p		J26	N32			LOW
B2	VREF1B2	IO	DIFFIO_TX62n		H26	N33			LOW
B2	VREF1B2	VREF1B2			M22	N29			
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO	DIFFIO_TX61p		G26	K34			LOW
B2	VREF1B2	IO	DIFFIO_TX61n		F26	K35			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO	DIFFIO_TX60p		F27	L35			LOW
B2	VREF1B2	IO	DIFFIO_TX60n		G27	L34			LOW
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO	DIFFIO_TX59p		H27	M34			LOW
B2	VREF1B2	IO	DIFFIO_TX59n		J27	M35			LOW
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO							LOW
B2	VREF1B2	IO	DIFFIO_TX58p		K27	N34			LOW
B2	VREF1B2	IO	DIFFIO_TX58n		L27	N35			LOW
B2	VREF1B2	IO	DIFFIO_RX57p		F28	K36			HIGH
B2	VREF1B2	IO	DIFFIO_RX57n		G28	K37			HIGH
B2	VREF1B2	IO	DIFFIO_TX57p		L24	P32			HIGH
B2	VREF1B2	IO	DIFFIO_TX57n		M24	P33			HIGH
B2	VREF2B2	IO	DIFFIO_RX56p		J28	J36			HIGH
B2	VREF2B2	IO	DIFFIO_RX56n		H28	J37			HIGH
B2	VREF2B2	IO	DIFFIO_TX56p		L25	P34			HIGH
B2	VREF2B2	IO	DIFFIO_TX56n		M25	P35			HIGH
B2	VREF2B2	IO	DIFFIO_RX55p		D29	L37			HIGH
B2	VREF2B2	IO	DIFFIO_RX55n		E29	L36			HIGH
B2	VREF2B2	IO	DIFFIO_TX55p		P24	R33			HIGH
B2	VREF2B2	IO	DIFFIO_TX55n		N24	R32			HIGH
B2	VREF2B2	IO	DIFFIO_RX54p		F29	K38			HIGH
B2	VREF2B2	IO	DIFFIO_RX54n		G29	K39			HIGH
B2	VREF2B2	IO	DIFFIO_TX54p		N25	R34			HIGH
B2	VREF2B2	IO	DIFFIO_TX54n		P25	R35			HIGH
B2	VREF2B2	IO	DIFFIO_RX53p		H29	M36			HIGH
B2	VREF2B2	IO	DIFFIO_RX53n		J29	M37			HIGH
B2	VREF2B2	IO	DIFFIO_TX53p		M26	T33			HIGH
B2	VREF2B2	IO	DIFFIO_TX53n		N26	T32			HIGH
B2	VREF2B2	IO	DIFFIO_RX52p		D30	L38			HIGH
B2	VREF2B2	IO	DIFFIO_RX52n		E30	L39			HIGH
B2	VREF2B2	IO	DIFFIO_TX52p		M27	T30			HIGH
B2	VREF2B2	IO	DIFFIO_TX52n		N27	T31			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF2B2	VREF2B2			N22	P29			
B2	VREF2B2	IO	DIFFIO_RX51p		F30	M38			HIGH
B2	VREF2B2	IO	DIFFIO_RX51n		G30	M39			HIGH
B2	VREF2B2	IO	DIFFIO_TX51p		P27	T34			HIGH
B2	VREF2B2	IO	DIFFIO_TX51n		R27	T35			HIGH
B2	VREF2B2	IO	DIFFIO_RX50p		H30	N36			HIGH
B2	VREF2B2	IO	DIFFIO_RX50n		J30	N37			HIGH
B2	VREF2B2	IO	DIFFIO_TX50p		R26	U35			HIGH
B2	VREF2B2	IO	DIFFIO_TX50n		P26	U34			HIGH
B2	VREF2B2	IO	DIFFIO_RX49p		F31	N38			HIGH
B2	VREF2B2	IO	DIFFIO_RX49n		G31	P38			HIGH
B2	VREF2B2	IO	DIFFIO_TX49p		N23	U33			HIGH
B2	VREF2B2	IO	DIFFIO_TX49n		P23	U32			HIGH
B2	VREF2B2	IO	DIFFIO_RX48p		H31	P39			HIGH
B2	VREF2B2	IO	DIFFIO_RX48n		J31	R38			HIGH
B2	VREF2B2	IO	DIFFIO_TX48p		T25	V35			HIGH
B2	VREF2B2	IO	DIFFIO_TX48n		R25	V34			HIGH
B2	VREF2B2	IO	DIFFIO_RX47p/RUP2		K28	P36			HIGH
B2	VREF2B2	IO	DIFFIO_RX47n/RDN2		K29	P37			HIGH
B2	VREF2B2	IO	DIFFIO_TX47p			U31			LOW
B2	VREF2B2	IO	DIFFIO_TX47n			U30			LOW
B2	VREF3B2	IO	DIFFIO_RX46p		M28	R36			HIGH
B2	VREF3B2	IO	DIFFIO_RX46n		L28	R37			HIGH
B2	VREF3B2	IO	DIFFIO_TX46p			U29			LOW
B2	VREF3B2	IO	DIFFIO_TX46n			U28			LOW
B2	VREF3B2	IO	DIFFIO_RX45p		M29	T36			HIGH
B2	VREF3B2	IO	DIFFIO_RX45n		L29	T37			HIGH
B2	VREF3B2	IO	DIFFIO_TX45p			V28			LOW
B2	VREF3B2	IO	DIFFIO_TX45n			V27			LOW
B2	VREF3B2	IO	DIFFIO_RX44p		P28	T39			HIGH
B2	VREF3B2	IO	DIFFIO_RX44n		N28	T38			HIGH
B2	VREF3B2	IO	DIFFIO_TX44p			V29			LOW
B2	VREF3B2	IO	DIFFIO_TX44n			V30			LOW
B2	VREF3B2	IO	DIFFIO_RX43p		N29	U36			HIGH
B2	VREF3B2	IO	DIFFIO_RX43n		P29	U37			HIGH
B2	VREF3B2	IO	DIFFIO_TX43p			V32			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF3B2	IO	DIFFIO_TX43n			V31			LOW
B2	VREF3B2	IO	DIFFIO_RX42p		L30	U38			HIGH
B2	VREF3B2	IO	DIFFIO_RX42n		K30	U39			HIGH
B2	VREF3B2	IO	DIFFIO_TX42p			V33			LOW
B2	VREF3B2	IO	DIFFIO_TX42n			W34			LOW
B2	VREF3B2	VREF3B2			P22	R29			
B2	VREF3B2	IO	DIFFIO_RX41p		N30	V36			HIGH
B2	VREF3B2	IO	DIFFIO_RX41n		M30	V37			HIGH
B2	VREF3B2	IO	DIFFIO_TX41p			V26			LOW
B2	VREF3B2	IO	DIFFIO_TX41n			W26			LOW
B2	VREF3B2	IO	DIFFIO_RX40p		L31	V38			HIGH
B2	VREF3B2	IO	DIFFIO_RX40n		K31	V39			HIGH
B2	VREF3B2	IO	DIFFIO_TX40p			W28			LOW
B2	VREF3B2	IO	DIFFIO_TX40n			W27			LOW
B2	VREF3B2	IO	DIFFIO_RX39p		R30	W39			HIGH
B2	VREF3B2	IO	DIFFIO_RX39n		P30	W38			HIGH
B2	VREF3B2	IO	DIFFIO_TX39p			W29			LOW
B2	VREF3B2	IO	DIFFIO_TX39n			W30			LOW
B2	VREF3B2	IO	DIFFIO_RX38p		P31	W37			HIGH
B2	VREF3B2	IO	DIFFIO_RX38n		R31	W36			HIGH
B2	VREF3B2	IO	DIFFIO_TX38p			W31			LOW
B2	VREF3B2	IO	DIFFIO_TX38n			W32			LOW
B2	VREF3B2	CLK0n			R28	Y39			
B2	VREF3B2	CLK0p			R29	Y38			
B2	VREF3B2	IO	CLK1n		T30	Y34			
B2	VREF3B2	CLK1p			T31	Y35			
		VCCINT							
		VCCA_PLL1			R24	AA32			
		GND							
		GNDA_PLL1			T24	Y31			
		VCCG_PLL1			R22	Y28			
		GNDG_PLL1			R23	Y29			
		VCCINT							
		VCCA_PLL2			U24	AA30			
		GND							
		GNDA_PLL2			V24	AA31			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCG_PLL2			U23	AA28			
		GNDG_PLL2			V23	AA29			
B1	VREF0B1	CLK2p			T29	Y37			
B1	VREF0B1	CLK2n			T28	Y36			
B1	VREF0B1	CLK3p			U29	AA35			
B1	VREF0B1	IO	CLK3n		U28	AA34			
B1	VREF0B1	IO	DIFFIO_RX37p		U31	AA39			HIGH
B1	VREF0B1	IO	DIFFIO_RX37n		V31	AA38			HIGH
B1	VREF0B1	IO	DIFFIO_TX37p			Y27			LOW
B1	VREF0B1	IO	DIFFIO_TX37n			Y26			LOW
B1	VREF0B1	IO	DIFFIO_RX36p		AB31	AA37			HIGH
B1	VREF0B1	IO	DIFFIO_RX36n		AA31	AA36			HIGH
B1	VREF0B1	IO	DIFFIO_TX36p			Y33			LOW
B1	VREF0B1	IO	DIFFIO_TX36n			AA33			LOW
B1	VREF0B1	IO	DIFFIO_RX35p		V30	AB38			HIGH
B1	VREF0B1	IO	DIFFIO_RX35n		U30	AB39			HIGH
B1	VREF0B1	IO	DIFFIO_TX35p			AA27			LOW
B1	VREF0B1	IO	DIFFIO_TX35n			AA26			LOW
B1	VREF0B1	IO	DIFFIO_RX34p		W30	AB37			HIGH
B1	VREF0B1	IO	DIFFIO_RX34n		Y30	AB36			HIGH
B1	VREF0B1	IO	DIFFIO_TX34p			AB33			LOW
B1	VREF0B1	IO	DIFFIO_TX34n			AB32			LOW
B1	VREF0B1	VREF0B1			V22	AE29			
B1	VREF0B1	IO	DIFFIO_RX33p		AA30	AC39			HIGH
B1	VREF0B1	IO	DIFFIO_RX33n		AB30	AC38			HIGH
B1	VREF0B1	IO	DIFFIO_TX33p			AB31			LOW
B1	VREF0B1	IO	DIFFIO_TX33n			AB30			LOW
B1	VREF0B1	IO	DIFFIO_RX32p		V29	AC37			HIGH
B1	VREF0B1	IO	DIFFIO_RX32n		W29	AC36			HIGH
B1	VREF0B1	IO	DIFFIO_TX32p			AB28			LOW
B1	VREF0B1	IO	DIFFIO_TX32n			AB29			LOW
B1	VREF0B1	IO	DIFFIO_RX31p		Y29	AD39			HIGH
B1	VREF0B1	IO	DIFFIO_RX31n		AA29	AD38			HIGH
B1	VREF0B1	IO	DIFFIO_TX31p			AB27			LOW
B1	VREF0B1	IO	DIFFIO_TX31n			AB26			LOW
B1	VREF0B1	IO	DIFFIO_RX30p		V28	AD37			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF0B1	IO	DIFFIO_RX30n		W28	AD36			HIGH
B1	VREF0B1	IO	DIFFIO_TX30p			AC26			LOW
B1	VREF0B1	IO	DIFFIO_TX30n			AC27			LOW
B1	VREF0B1	IO	DIFFIO_RX29p		Y28	AE37			HIGH
B1	VREF0B1	IO	DIFFIO_RX29n		AA28	AE36			HIGH
B1	VREF0B1	IO	DIFFIO_TX29p			AC28			LOW
B1	VREF0B1	IO	DIFFIO_TX29n			AC29			LOW
B1	VREF1B1	IO	DIFFIO_RX28p/RUP1		AB29	AF37			HIGH
B1	VREF1B1	IO	DIFFIO_RX28n/RDN1		AB28	AF36			HIGH
B1	VREF1B1	IO	DIFFIO_TX28p			AC31			LOW
B1	VREF1B1	IO	DIFFIO_TX28n			AC30			LOW
B1	VREF1B1	IO	DIFFIO_RX27p		AC31	AE38			HIGH
B1	VREF1B1	IO	DIFFIO_RX27n		AD31	AF39			HIGH
B1	VREF1B1	IO	DIFFIO_TX27p		V25	AB34			HIGH
B1	VREF1B1	IO	DIFFIO_TX27n		U25	AB35			HIGH
B1	VREF1B1	IO	DIFFIO_RX26p		AE31	AF38			HIGH
B1	VREF1B1	IO	DIFFIO_RX26n		AF31	AG38			HIGH
B1	VREF1B1	IO	DIFFIO_TX26p		U26	AC32			HIGH
B1	VREF1B1	IO	DIFFIO_TX26n		T26	AC33			HIGH
B1	VREF1B1	IO	DIFFIO_RX25p		AC30	AG37			HIGH
B1	VREF1B1	IO	DIFFIO_RX25n		AD30	AG36			HIGH
B1	VREF1B1	IO	DIFFIO_TX25p		T27	AC34			HIGH
B1	VREF1B1	IO	DIFFIO_TX25n		U27	AC35			HIGH
B1	VREF1B1	IO	DIFFIO_RX24p		AF30	AH39			HIGH
B1	VREF1B1	IO	DIFFIO_RX24n		AE30	AH38			HIGH
B1	VREF1B1	IO	DIFFIO_TX24p		V26	AD34			HIGH
B1	VREF1B1	IO	DIFFIO_TX24n		W26	AD35			HIGH
B1	VREF1B1	VREF1B1			W22	AF29			
B1	VREF1B1	IO	DIFFIO_RX23p		AG30	AH37			HIGH
B1	VREF1B1	IO	DIFFIO_RX23n		AH30	AH36			HIGH
B1	VREF1B1	IO	DIFFIO_TX23p		W24	AD33			HIGH
B1	VREF1B1	IO	DIFFIO_TX23n		Y24	AD32			HIGH
B1	VREF1B1	IO	DIFFIO_RX22p		AC29	AJ39			HIGH
B1	VREF1B1	IO	DIFFIO_RX22n		AD29	AJ38			HIGH
B1	VREF1B1	IO	DIFFIO_TX22p		W25	AD31			HIGH
B1	VREF1B1	IO	DIFFIO_TX22n		Y25	AD30			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_RX21p		AE29	AJ37			HIGH
B1	VREF1B1	IO	DIFFIO_RX21n		AF29	AJ36			HIGH
B1	VREF1B1	IO	DIFFIO_TX21p		Y26	AE35			HIGH
B1	VREF1B1	IO	DIFFIO_TX21n		AA26	AE34			HIGH
B1	VREF1B1	IO	DIFFIO_RX20p		AH29	AK38			HIGH
B1	VREF1B1	IO	DIFFIO_RX20n		AG29	AK39			HIGH
B1	VREF1B1	IO	DIFFIO_TX20p		W23	AE33			HIGH
B1	VREF1B1	IO	DIFFIO_TX20n		Y23	AE32			HIGH
B1	VREF1B1	IO	DIFFIO_RX19p		AC28	AK37			HIGH
B1	VREF1B1	IO	DIFFIO_RX19n		AD28	AK36			HIGH
B1	VREF1B1	IO	DIFFIO_TX19p		V27	AF35			HIGH
B1	VREF1B1	IO	DIFFIO_TX19n		W27	AF34			HIGH
B1	VREF2B1	IO	DIFFIO_RX18p		AE28	AL37			HIGH
B1	VREF2B1	IO	DIFFIO_RX18n		AF28	AL36			HIGH
B1	VREF2B1	IO	DIFFIO_TX18p		Y27	AF33			HIGH
B1	VREF2B1	IO	DIFFIO_TX18n		AA27	AF32			HIGH
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO	DIFFIO_TX17p		AB27	AG35			LOW
B1	VREF2B1	IO	DIFFIO_TX17n		AC27	AG34			LOW
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO	DIFFIO_TX16p		AE27	AG33			LOW
B1	VREF2B1	IO	DIFFIO_TX16n		AD27	AG32			LOW
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO	DIFFIO_TX15p		AG27	AH34			LOW
B1	VREF2B1	IO	DIFFIO_TX15n		AF27	AH35			LOW
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO							LOW
B1	VREF2B1	IO	DIFFIO_TX14p		AB26	AK35			LOW
B1	VREF2B1	IO	DIFFIO_TX14n		AC26	AK34			LOW
B1	VREF2B1	VREF2B1			Y22	AG29			
B1	VREF2B1	IO	DIFFIO_RX13p			AM39			LOW
B1	VREF2B1	IO	DIFFIO_RX13n			AM38			LOW
B1	VREF2B1	IO	DIFFIO_TX13p		AD26	AH33			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF2B1	IO	DIFFIO_TX13n		AE26	AH32			LOW
B1	VREF2B1	IO	DIFFIO_RX12p			AN39			LOW
B1	VREF2B1	IO	DIFFIO_RX12n			AN38			LOW
B1	VREF2B1	IO	DIFFIO_TX12p		AA25	AJ35			LOW
B1	VREF2B1	IO	DIFFIO_TX12n		AB25	AJ34			LOW
B1	VREF2B1	IO	DIFFIO_RX11p			AP38			LOW
B1	VREF2B1	IO	DIFFIO_RX11n			AP39			LOW
B1	VREF2B1	IO	DIFFIO_TX11p		AD25	AJ33			LOW
B1	VREF2B1	IO	DIFFIO_TX11n		AC25	AJ32			LOW
B1	VREF2B1	IO	DIFFIO_RX10p			AR38			LOW
B1	VREF2B1	IO	DIFFIO_RX10n			AR39			LOW
B1	VREF2B1	IO	DIFFIO_TX10p		AA24	AK32			LOW
B1	VREF2B1	IO	DIFFIO_TX10n		AB24	AK33			LOW
B1	VREF2B1	IO	DIFFIO_RX9p			AT39			LOW
B1	VREF2B1	IO	DIFFIO_RX9n			AT38			LOW
B1	VREF2B1	IO	DIFFIO_TX9p		AD24	AL33			LOW
B1	VREF2B1	IO	DIFFIO_TX9n		AC24	AL32			LOW
B1	VREF3B1	IO	DIFFIO_RX8p			AM37			LOW
B1	VREF3B1	IO	DIFFIO_RX8n			AM36			LOW
B1	VREF3B1	IO	DIFFIO_TX8p		AE25	AH31			LOW
B1	VREF3B1	IO	DIFFIO_TX8n		AF25	AH30			LOW
B1	VREF3B1	IO	DIFFIO_RX7p			AN37			LOW
B1	VREF3B1	IO	DIFFIO_RX7n			AN36			LOW
B1	VREF3B1	IO	DIFFIO_TX7p			AE31			LOW
B1	VREF3B1	IO	DIFFIO_TX7n			AE30			LOW
B1	VREF3B1	IO	DIFFIO_RX6p			AP36			LOW
B1	VREF3B1	IO	DIFFIO_RX6n			AP37			LOW
B1	VREF3B1	IO	DIFFIO_TX6p			AF30			LOW
B1	VREF3B1	IO	DIFFIO_TX6n			AF31			LOW
B1	VREF3B1	IO	DIFFIO_RX5p			AR37			LOW
B1	VREF3B1	IO	DIFFIO_RX5n			AR36			LOW
B1	VREF3B1	IO	DIFFIO_TX5p			AG30			LOW
B1	VREF3B1	IO	DIFFIO_TX5n			AG31			LOW
B1	VREF3B1	IO	DIFFIO_RX4p			AU38			LOW
B1	VREF3B1	IO	DIFFIO_RX4n			AT37			LOW
B1	VREF3B1	IO	DIFFIO_TX4p			AD29			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF3B1	IO	DIFFIO_TX4n			AD28			LOW
B1	VREF3B1	VREF3B1			AA22	AH29			
B1	VREF3B1	IO	DIFFIO_RX3p			AL35			LOW
B1	VREF3B1	IO	DIFFIO_RX3n			AL34			LOW
B1	VREF3B1	IO	DIFFIO_TX3p			AD27			LOW
B1	VREF3B1	IO	DIFFIO_TX3n			AD26			LOW
B1	VREF3B1	IO	DIFFIO_RX2p			AM35			LOW
B1	VREF3B1	IO	DIFFIO_RX2n			AM34			LOW
B1	VREF3B1	IO	DIFFIO_TX2p			AE28			LOW
B1	VREF3B1	IO	DIFFIO_TX2n			AE27			LOW
B1	VREF3B1	IO	DIFFIO_RX1p			AN34			LOW
B1	VREF3B1	IO	DIFFIO_RX1n			AN35			LOW
B1	VREF3B1	IO	DIFFIO_TX1p			AF28			LOW
B1	VREF3B1	IO	DIFFIO_TX1n			AF27			LOW
B1	VREF3B1	IO	DIFFIO_RX0p			AP35			LOW
B1	VREF3B1	IO	DIFFIO_RX0n			AP34			LOW
B1	VREF3B1	IO	DIFFIO_TX0p			AF26			LOW
B1	VREF3B1	IO	DIFFIO_TX0n			AE26			LOW
B1	VREF3B1	FPLL8CLKn			AG31	AL38			
B1	VREF3B1	FPLL8CLKp			AH31	AL39			
B1	VREF3B1	IO				AG28			
B1	VREF3B1	IO				AH28			
		VCCINT							
		VCCA_PLL8			AB23	AJ30			
		GND							
		GNDA_PLL8			AA23	AJ31			
		VCCG_PLL8			AD23	AL31			
		GNDG_PLL8			AC23	AK31			
B8	VREF0B8	IO							
B8	VREF0B8	IO				AR35			
B8	VREF0B8	IO				AT36			
B8	VREF0B8	IO			AG28	AN32			
B8	VREF0B8	IO				AR34			
B8	VREF0B8	IO				AU36			
B8	VREF0B8	IO				AN33			
B8	VREF0B8	IO				AL30			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF0B8	IO				AM31			
B8	VREF0B8	IO			AF26	AT35			
B8	VREF0B8	IO	DQ9B7		AK29	AV34	DQ3B15	DQ1B31	
B8	VREF0B8	IO				AN31			
B8	VREF0B8	IO	DQ9B6		AJ29	AU34	DQ3B14	DQ1B30	
B8	VREF0B8	IO				AP33			
B8	VREF0B8	IO	DQ9B5		AJ28	AU33	DQ3B13	DQ1B29	
B8	VREF0B8	IO			AE24	AV37			
B8	VREF0B8	IO	DQ9B4		AL28	AW33	DQ3B12	DQ1B28	
B8	VREF0B8	IO				AR33			
B8	VREF0B8	VREF0B8			AB22	AJ29			
B8	VREF0B8	IO	DQ9B3		AH27	AW34	DQ3B11	DQ1B27	
B8	VREF0B8	IO				AK29			
B8	VREF0B8	IO	DQS9B		AK28	AV33			
B8	VREF0B8	IO			AJ30	AP32			
B8	VREF0B8	IO	DQ9B2		AL27	AV32	DQ3B10	DQ1B26	
B8	VREF0B8	IO				AV35			
B8	VREF0B8	IO	DQ9B1		AJ27	AU32	DQ3B9	DQ1B25	
B8	VREF0B8	IO				AL29			
B8	VREF0B8	IO	DQ9B0		AK27	AW32	DQ3B8	DQ1B24	
B8	VREF0B8	IO			AH28	AT34			
B8	VREF0B8	IO				AV36			
B8	VREF0B8	IO				AP31			
B8	VREF1B8	IO				AK28			
B8	VREF1B8	IO				AU35			
B8	VREF1B8	IO				AT33			
B8	VREF1B8	IO				AL28			
B8	VREF1B8	IO				AN30			
B8	VREF1B8	IO	DQ8B7		AH26	AU31	DQ3B7	DQ1B23	
B8	VREF1B8	IO				AM29			
B8	VREF1B8	IO	DQ8B6		AG26	AV31	DQ3B6	DQ1B22	
B8	VREF1B8	IO			AD22	AR32			
B8	VREF1B8	IO	DQ8B5		AK26	AW31	DQ3B5	DQ1B21	
B8	VREF1B8	IO				AP30			
B8	VREF1B8	IO	DQ8B4		AL26	AW30	DQ3B4	DQ1B20	
B8	VREF1B8	IO				AK27			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF1B8	IO	DQ8B3		AH25	AU30	DQ3B3	DQ1B19	
B8	VREF1B8	IO			AC22	AW36			
B8	VREF1B8	IO	DQS8B		AJ26	AV30	DQS3B		
B8	VREF1B8	IO				AM28			
B8	VREF1B8	IO	DQ8B2		AK25	AU29	DQ3B2	DQ1B18	
B8	VREF1B8	VREF1B8			AB21	AJ28			
B8	VREF1B8	IO				AH27			
B8	VREF1B8	IO	DQ8B1		AJ25	AV29	DQ3B1	DQ1B17	
B8	VREF1B8	IO			AD21	AL27			
B8	VREF1B8	IO	DQ8B0		AL25	AW29	DQ3B0	DQ1B16	
B8	VREF1B8	IO			AE22	AT32			
B8	VREF1B8	IO				AN28			
B8	VREF1B8	IO				AG27			
B8	VREF1B8	IO				AN29			
B8	VREF1B8	IO				AR31			
B8	VREF1B8	IO				AW35			
B8	VREF1B8	IO				AR30			
B8	VREF1B8	IO				AM27			
B8	VREF2B8	IO	DQ7B7		AG24	AR28	DQ2B15	DQ1B15	
B8	VREF2B8	IO				AK26			
B8	VREF2B8	IO	DQ7B6		AH23	AT28	DQ2B14	DQ1B14	
B8	VREF2B8	IO			AC21	AL26			
B8	VREF2B8	IO	DQ7B5		AK24	AU28	DQ2B13	DQ1B13	
B8	VREF2B8	IO				AT31			
B8	VREF2B8	IO	DQ7B4		AH24	AV28	DQ2B12	DQ1B12	
B8	VREF2B8	IO			AA21	AH26			
B8	VREF2B8	IO	DQ7B3		AJ23	AR27	DQ2B11	DQ1B11	
B8	VREF2B8	IO				AP29			
B8	VREF2B8	IO	DQS7B		AJ24	AT27		DQS1B	
B8	VREF2B8	IO				AP28			
B8	VREF2B8	IO	DQ7B2		AL24	AW28	DQ2B10	DQ1B10	
B8	VREF2B8	IO			AD20	AG26			
B8	VREF2B8	IO	DQ7B1		AK23	AU27	DQ2B9	DQ1B9	
B8	VREF2B8	IO				AR29			
B8	VREF2B8	IO	DQ7B0		AL23	AV27	DQ2B8	DQ1B8	
B8	VREF2B8	IO				AP27			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF2B8	VREF2B8			AB20	AJ27			
B8	VREF2B8	IO				AG25			
B8	VREF2B8	IO				AH25			
B8	VREF2B8	IO				AT30			
B8	VREF2B8	IO				AM26			
B8	VREF2B8	IO	FCLK3		AF23	AT29			
B8	VREF2B8	IO	FCLK2		AF22	AN26			
B8	VREF2B8	IO				AK25			
B8	VREF2B8	IO	DQ6B7		AG22	AR26	DQ2B7	DQ1B7	
B8	VREF2B8	IO				AN27			
B8	VREF2B8	IO	DQ6B6		AH22	AT26	DQ2B6	DQ1B6	
B8	VREF2B8	IO				AP26			
B8	VREF2B8	IO	DQ6B5		AK22	AU26	DQ2B5	DQ1B5	
B8	VREF3B8	IO				AF25			
B8	VREF3B8	IO	DQ6B4		AG21	AV26	DQ2B4	DQ1B4	
B8	VREF3B8	IO		PGM2	AF24	AL25			
B8	VREF3B8	IO	DQ6B3		AH21	AW26	DQ2B3	DQ1B3	
B8	VREF3B8	IO				AM25			
B8	VREF3B8	IO	DQS6B		AJ22	AU25	DQS2B		
B8	VREF3B8	IO				AF24			
B8	VREF3B8	IO	DQ6B2		AL22	AT25	DQ2B2	DQ1B2	
B8	VREF3B8	IO			AE21	AN25			
B8	VREF3B8	IO	DQ6B1		AJ21	AR25	DQ2B1	DQ1B1	
B8	VREF3B8	IO				AP25			
B8	VREF3B8	IO	DQ6B0		AK21	AV25	DQ2B0	DQ1B0	
B8	VREF3B8	IO	RDN8		AE23	AH24			
B8	VREF3B8	IO	RUP8		AG25	AF23			
B8	VREF3B8	IO				AJ24			
B8	VREF3B8	IO				AL24			
B8	VREF3B8	IO				AN24			
B8	VREF3B8	IO				AM24			
B8	VREF3B8	VREF3B8			AB19	AJ26			
B8	VREF3B8	IO				AG24			
B8	VREF3B8	IO			AC20	AK24			
B8	VREF3B8	IO	DQ5B7		AG20	AT24			
B8	VREF3B8	IO				AP24			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF3B8	IO	DQ5B6		AH20	AU24			
B8	VREF3B8	IO			AE20	AR24			
B8	VREF3B8	IO	DQ5B5		AK20	AV24			
B8	VREF3B8	IO			AD19	AG23			
B8	VREF3B8	IO	DQ5B4		AL20	AW24			
B8	VREF3B8	IO		RDYnBSY	AG23	AH23			
B8	VREF3B8	IO	DQ5B3		AG19	AW23			
B8	VREF3B8	IO				AP23			
B8	VREF4B8	IO	DQS5B		AJ20	AU23			
B8	VREF4B8	IO			AC19	AK23			
B8	VREF4B8	IO	DQ5B2		AH19	AR23			
B8	VREF4B8	IO		nCS	AF20	AL23			
B8	VREF4B8	IO	DQ5B1		AJ19	AV23			
B8	VREF4B8	IO			AE18	AM23			
B8	VREF4B8	IO	DQ5B0		AK19	AT23			
B8	VREF4B8	IO				AF22			
B8	VREF4B8	IO		CS	AF21	AJ23			
B8	VREF4B8	IO			AE19	AG22			
B8	VREF4B8	IO				AN23			
B8	VREF4B8	IO				AR22			
B8	VREF4B8	IO				AH22			
B8	VREF4B8	IO				AF21			
B8	VREF4B8	IO			AA19	AJ22			
B8	VREF4B8	IO				AL22			
B8	VREF4B8	IO				AP22			
B8	VREF4B8	IO				AN22			
B8	VREF4B8	VREF4B8			AB18	AJ25			
B8	VREF4B8	IO	CLK5n		AH18	AU22			
B8	VREF4B8	CLK5p			AJ18	AT22			
B8	VREF4B8	IO	CLK4n		AK18	AW22			
B8	VREF4B8	CLK4p			AL18	AV22			
B8	VREF4B8	PLL_ENA		PLL_ENA	AF19	AM22			
B8	VREF4B8	MSEL0		MSEL0	AF18	AP21			
B8	VREF4B8	MSEL1		MSEL1	AG18	AG21			
B8	VREF4B8	MSEL2		MSEL2	AG17	AM21			
B12	VREF4B8	IO	PLL6_OUT3n		AL17	AV20			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B12	VREF4B8	IO	PLL6_OUT3p		AK17	AW20			
B12	VREF4B8	IO	PLL6_OUT2n		AJ17	AW21			
B12	VREF4B8	IO	PLL6_OUT2p		AH17	AV21			
B11	VREF4B8	IO	PLL6_FBn		AJ15	AU20			
B11	VREF4B8	IO	PLL6_FBp		AH15	AT20			
B11	VREF4B8	IO	PLL6_OUT1n		AL15	AU21			
B11	VREF4B8	IO	PLL6_OUT1p		AK15	AT21			
B11	VREF4B8	IO	PLL6_OUT0n		AL16	AU19			
B11	VREF4B8	IO	PLL6_OUT0p		AK16	AT19			
B12		VCC_PLL6_OUTB			AC18	AH21			
B12		VCC_PLL6_OUTB							
B11		VCC_PLL6_OUTA			AD17	AJ21			
B11		VCC_PLL6_OUTA							
		VCCINT							
		VCCA_PLL6			AB17	AK21			
		GND							
		GNDA_PLL6			AC17	AL20			
		VCCG_PLL6			AD15	AJ20			
		GNDG_PLL6			AD16	AH20			
		VCCINT							
		VCCA_PLL12			AC14	AK19			
		GND							
		GNDA_PLL12			AD14	AL19			
		VCCG_PLL12			AC15	AJ19			
		GNDG_PLL12			AB15	AH19			
B7	VREF0B7	CLK7p			AJ14	AW18			
B7	VREF0B7	IO	CLK7n		AH14	AV18			
B7	VREF0B7	CLK6p			AL14	AW19			
B7	VREF0B7	IO	CLK6n/PLL12_OUT		AK14	AV19			
B7	VREF0B7	nCE		nCE	AF17	AN20			
B7	VREF0B7	nCEO		nCEO	AF16	AP20			
B7	VREF0B7	IO				AF20			
B7	VREF0B7	IO				AG19			
B7	VREF0B7	IO		PGM0	AE17	AG20			
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	AE16	AR20			
B7	VREF0B7	VCCSEL		VCCSEL	AE15	AM19			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF0B7	PORSEL		PORSEL	AG16	AN19			
B7	VREF0B7	IO				AK18			
B7	VREF0B7	IO				AF19			
B7	VREF0B7	IO		INIT_DONE	AF15	AL18			
B7	VREF0B7	IO				AM18			
B7	VREF0B7	IO				AP19			
B7	VREF0B7	IO				AR19			
B7	VREF0B7	VREF0B7			AB14	AJ15			
B7	VREF0B7	IO				AH18			
B7	VREF0B7	IO				AG18			
B7	VREF0B7	IO				AJ18			
B7	VREF0B7	IO			AH16	AP18			
B7	VREF0B7	IO				AN18			
B7	VREF0B7	IO				AR18			
B7	VREF0B7	IO				AG17			
B7	VREF0B7	IO				AH17			
B7	VREF0B7	IO			AA16	AF18			
B7	VREF0B7	IO		nRS	AE14	AL17			
B7	VREF0B7	IO				AT18			
B7	VREF0B7	IO	DQ4B7		AK13	AU17			
B7	VREF0B7	IO			AA15	AJ17			
B7	VREF0B7	IO	DQ4B6		AG13	AR17			
B7	VREF0B7	IO		RUnLU	AJ16	AK17			
B7	VREF0B7	IO	DQ4B5		AH13	AT17			
B7	VREF0B7	IO				AU18			
B7	VREF0B7	IO	DQ4B4		AJ13	AV17			
B7	VREF1B7	IO			AC13	AF17			
B7	VREF1B7	IO	DQ4B3		AK12	AV16			
B7	VREF1B7	IO		PGM1	AG15	AF16			
B7	VREF1B7	IO	DQS4B		AJ12	AU16			
B7	VREF1B7	IO			AD13	AM17			
B7	VREF1B7	IO	DQ4B2		AL12	AW17			
B7	VREF1B7	IO				AG16			
B7	VREF1B7	IO	DQ4B1		AG12	AT16			
B7	VREF1B7	IO	DEV_CLRn		AF14	AN17			
B7	VREF1B7	IO	DQ4B0		AH12	AW16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF1B7	IO			AE13	AM16			
B7	VREF1B7	IO				AP16			
B7	VREF1B7	VREF1B7			AB13	AJ14			
B7	VREF1B7	IO				AK16			
B7	VREF1B7	IO				AH16			
B7	VREF1B7	IO				AL16			
B7	VREF1B7	IO				AJ16			
B7	VREF1B7	IO	RDN7		AG14	AP17			
B7	VREF1B7	IO	RUP7		AF13	AN16			
B7	VREF1B7	IO	DQ3B7		AL10	AT15	DQ1B15	DQ0B31	
B7	VREF1B7	IO				AF15			
B7	VREF1B7	IO	DQ3B6		AJ11	AR15	DQ1B14	DQ0B30	
B7	VREF1B7	IO				AP15			
B7	VREF1B7	IO	DQ3B5		AK11	AV15	DQ1B13	DQ0B29	
B7	VREF1B7	IO			AA13	AR16			
B7	VREF1B7	IO	DQ3B4		AG11	AV14	DQ1B12	DQ0B28	
B7	VREF1B7	IO			AC12	AG15			
B7	VREF1B7	IO	DQ3B3		AH11	AW14	DQ1B11	DQ0B27	
B7	VREF1B7	IO				AM15			
B7	VREF1B7	IO	DQS3B		AJ10	AU15	DQS1B		
B7	VREF1B7	IO			AA11	AN15			
B7	VREF2B7	IO	DQ3B2		AG10	AR14	DQ1B10	DQ0B26	
B7	VREF2B7	IO				AK15			
B7	VREF2B7	IO	DQ3B1		AH10	AT14	DQ1B9	DQ0B25	
B7	VREF2B7	IO				AL15			
B7	VREF2B7	IO	DQ3B0		AK10	AU14	DQ1B8	DQ0B24	
B7	VREF2B7	IO				AP14			
B7	VREF2B7	IO				AH15			
B7	VREF2B7	IO				AG14			
B7	VREF2B7	IO				AM14			
B7	VREF2B7	IO				AR11			
B7	VREF2B7	IO	FCLK5		AF12	AN14			
B7	VREF2B7	IO	FCLK4		AF11	AT11			
B7	VREF2B7	VREF2B7			AB12	AJ13			
B7	VREF2B7	IO				AH14			
B7	VREF2B7	IO	DQ2B7		AL8	AT13	DQ1B7	DQ0B23	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF2B7	IO			AD12	AP12			
B7	VREF2B7	IO	DQ2B6		AK9	AU13	DQ1B6	DQ0B22	
B7	VREF2B7	IO				AP13			
B7	VREF2B7	IO	DQ2B5		AL9	AV13	DQ1B5	DQ0B21	
B7	VREF2B7	IO			AC11	AG13			
B7	VREF2B7	IO	DQ2B4		AH8	AV12	DQ1B4	DQ0B20	
B7	VREF2B7	IO			AE12	AN12			
B7	VREF2B7	IO	DQ2B3		AK8	AR13	DQ1B3	DQ0B19	
B7	VREF2B7	IO				AN13			
B7	VREF2B7	IO	DQS2B		AJ8	AU12		DQS0B	
B7	VREF2B7	IO			AD11	AK14			
B7	VREF2B7	IO	DQ2B2		AG8	AR12	DQ1B2	DQ0B18	
B7	VREF2B7	IO			AE11	AL14			
B7	VREF2B7	IO	DQ2B1		AH9	AT12	DQ1B1	DQ0B17	
B7	VREF2B7	IO				AT10			
B7	VREF2B7	IO	DQ2B0		AJ9	AW12	DQ1B0	DQ0B16	
B7	VREF3B7	IO				AR9			
B7	VREF3B7	IO				AH13			
B7	VREF3B7	IO			AF10	AR10			
B7	VREF3B7	IO				AT8			
B7	VREF3B7	IO				AM13			
B7	VREF3B7	IO				AP11			
B7	VREF3B7	IO				AM12			
B7	VREF3B7	IO			AC10	AH12			
B7	VREF3B7	IO	DQ1B7		AK7	AV11	DQ0B15	DQ0B15	
B7	VREF3B7	IO				AL13			
B7	VREF3B7	IO	DQ1B6		AL7	AW11	DQ0B14	DQ0B14	
B7	VREF3B7	IO			AG9	AT9			
B7	VREF3B7	VREF3B7			AB11	AJ12			
B7	VREF3B7	IO	DQ1B5		AH6	AU10	DQ0B13	DQ0B13	
B7	VREF3B7	IO			AG7	AK13			
B7	VREF3B7	IO	DQ1B4		AK6	AW10	DQ0B12	DQ0B12	
B7	VREF3B7	IO			AE10	AW5			
B7	VREF3B7	IO	DQ1B3		AL6	AU11	DQ0B11	DQ0B11	
B7	VREF3B7	IO				AN11			
B7	VREF3B7	IO	DQS1B		AJ6	AV10	DQS0B		

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF3B7	IO			AD10	AM11			
B7	VREF3B7	IO	DQ1B2		AH7	AW9	DQ0B10	DQ0B10	
B7	VREF3B7	IO			AF9	AR8			
B7	VREF3B7	IO	DQ1B1		AJ7	AV9	DQ0B9	DQ0B9	
B7	VREF3B7	IO				AP10			
B7	VREF3B7	IO	DQ1B0		AG6	AU9	DQ0B8	DQ0B8	
B7	VREF3B7	IO				AK12			
B7	VREF3B7	IO				AL12			
B7	VREF3B7	IO				AT7			
B7	VREF3B7	IO				AW4			
B7	VREF3B7	IO				AN10			
B7	VREF4B7	IO				AL11			
B7	VREF4B7	IO				AK11			
B7	VREF4B7	IO			AE9	AV4			
B7	VREF4B7	IO	DQ0B7		AL4	AV8	DQ0B7	DQ0B7	
B7	VREF4B7	IO				AP9			
B7	VREF4B7	IO	DQ0B6		AL5	AW8	DQ0B6	DQ0B6	
B7	VREF4B7	IO			AJ2	AU4			
B7	VREF4B7	IO	DQ0B5		AJ4	AW6	DQ0B5	DQ0B5	
B7	VREF4B7	IO			AH4	AR7			
B7	VREF4B7	IO	DQ0B4		AK3	AU8	DQ0B4	DQ0B4	
B7	VREF4B7	IO				AV5			
B7	VREF4B7	IO	DQ0B3		AK5	AW7	DQ0B3	DQ0B3	
B7	VREF4B7	VREF4B7			AB10	AJ11			
B7	VREF4B7	IO			AG4	AR6			
B7	VREF4B7	IO	DQS0B		AK4	AV7			
B7	VREF4B7	IO				AP8			
B7	VREF4B7	IO	DQ0B2		AH5	AU7	DQ0B2	DQ0B2	
B7	VREF4B7	IO			AF8	AU5			
B7	VREF4B7	IO	DQ0B1		AJ5	AV6	DQ0B1	DQ0B1	
B7	VREF4B7	IO				AL10			
B7	VREF4B7	IO	DQ0B0		AJ3	AU6	DQ0B0	DQ0B0	
B7	VREF4B7	IO			AE8	AT5			
B7	VREF4B7	IO				AM9			
B7	VREF4B7	IO				AN9			
B7	VREF4B7	IO				AV3			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF4B7	IO				AR5			
B7	VREF4B7	IO				AN7			
B7	VREF4B7	IO			AF6	AN8			
B7	VREF4B7	IO				AT4			
B7	VREF4B7	IO				AT6			
B7	VREF4B7	IO				AP7			
		GNDG_PLL9			AC9	AK9			
		VCCG_PLL9			AD9	AL9			
		GNDA_PLL9			AA9	AJ9			
		GND							
		VCCA_PLL9			AB9	AJ10			
		VCCINT							
B6	VREF0B6	IO				AF13			
B6	VREF0B6	IO				AF14			
B6	VREF0B6	FPLL9CLKp			AH1	AL1			
B6	VREF0B6	FPLL9CLKn			AG1	AL2			
B6	VREF0B6	IO	DIFFIO_TX151n			AF12			LOW
B6	VREF0B6	IO	DIFFIO_TX151p			AG12			LOW
B6	VREF0B6	IO	DIFFIO_RX151n			AP6			LOW
B6	VREF0B6	IO	DIFFIO_RX151p			AP5			LOW
B6	VREF0B6	IO	DIFFIO_TX150n			AE12			LOW
B6	VREF0B6	IO	DIFFIO_TX150p			AE13			LOW
B6	VREF0B6	IO	DIFFIO_RX150n			AN5			LOW
B6	VREF0B6	IO	DIFFIO_RX150p			AN6			LOW
B6	VREF0B6	IO	DIFFIO_TX149n			AG10			LOW
B6	VREF0B6	IO	DIFFIO_TX149p			AG9			LOW
B6	VREF0B6	IO	DIFFIO_RX149n			AM6			LOW
B6	VREF0B6	IO	DIFFIO_RX149p			AM5			LOW
B6	VREF0B6	IO	DIFFIO_TX148n			AF10			LOW
B6	VREF0B6	IO	DIFFIO_TX148p			AF9			LOW
B6	VREF0B6	IO	DIFFIO_RX148n			AL6			LOW
B6	VREF0B6	IO	DIFFIO_RX148p			AL5			LOW
B6	VREF0B6	VREF0B6			V10	AE11			
B6	VREF0B6	IO	DIFFIO_TX147n			AE14			LOW
B6	VREF0B6	IO	DIFFIO_TX147p			AD14			LOW
B6	VREF0B6	IO	DIFFIO_RX147n			AR4			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF0B6	IO	DIFFIO_RX147p			AR3			LOW
B6	VREF0B6	IO	DIFFIO_TX146n			AE9			LOW
B6	VREF0B6	IO	DIFFIO_TX146p			AE10			LOW
B6	VREF0B6	IO	DIFFIO_RX146n			AT3			LOW
B6	VREF0B6	IO	DIFFIO_RX146p			AU2			LOW
B6	VREF0B6	IO	DIFFIO_TX145n			AC13			LOW
B6	VREF0B6	IO	DIFFIO_TX145p			AD13			LOW
B6	VREF0B6	IO	DIFFIO_RX145n			AP3			LOW
B6	VREF0B6	IO	DIFFIO_RX145p			AP4			LOW
B6	VREF0B6	IO	DIFFIO_TX144n			AD12			LOW
B6	VREF0B6	IO	DIFFIO_TX144p			AD11			LOW
B6	VREF0B6	IO	DIFFIO_RX144n			AN4			LOW
B6	VREF0B6	IO	DIFFIO_RX144p			AN3			LOW
B6	VREF0B6	IO	DIFFIO_TX143n		AC8	AH10			LOW
B6	VREF0B6	IO	DIFFIO_TX143p		AD8	AH9			LOW
B6	VREF0B6	IO	DIFFIO_RX143n			AM4			LOW
B6	VREF0B6	IO	DIFFIO_RX143p			AM3			LOW
B6	VREF1B6	IO	DIFFIO_TX142n		AF7	AL8			LOW
B6	VREF1B6	IO	DIFFIO_TX142p		AE7	AL7			LOW
B6	VREF1B6	IO	DIFFIO_RX142n			AT2			LOW
B6	VREF1B6	IO	DIFFIO_RX142p			AT1			LOW
B6	VREF1B6	IO	DIFFIO_TX141n		AB8	AK7			LOW
B6	VREF1B6	IO	DIFFIO_TX141p		AA8	AK8			LOW
B6	VREF1B6	IO	DIFFIO_RX141n			AR2			LOW
B6	VREF1B6	IO	DIFFIO_RX141p			AR1			LOW
B6	VREF1B6	IO	DIFFIO_TX140n		AC7	AJ7			LOW
B6	VREF1B6	IO	DIFFIO_TX140p		AD7	AJ8			LOW
B6	VREF1B6	IO	DIFFIO_RX140n			AP1			LOW
B6	VREF1B6	IO	DIFFIO_RX140p			AP2			LOW
B6	VREF1B6	IO	DIFFIO_TX139n		AB7	AH8			LOW
B6	VREF1B6	IO	DIFFIO_TX139p		AA7	AH7			LOW
B6	VREF1B6	IO	DIFFIO_RX139n			AN2			LOW
B6	VREF1B6	IO	DIFFIO_RX139p			AN1			LOW
B6	VREF1B6	IO	DIFFIO_TX138n		AE6	AG8			LOW
B6	VREF1B6	IO	DIFFIO_TX138p		AD6	AG7			LOW
B6	VREF1B6	IO	DIFFIO_RX138n			AM2			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF1B6	IO	DIFFIO_RX138p			AM1			LOW
B6	VREF1B6	VREF1B6			W10	AF11			
B6	VREF1B6	IO	DIFFIO_TX137n		AC6	AK6			LOW
B6	VREF1B6	IO	DIFFIO_TX137p		AB6	AK5			LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO	DIFFIO_TX136n		AF5	AJ5			LOW
B6	VREF1B6	IO	DIFFIO_TX136p		AG5	AJ6			LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO	DIFFIO_TX135n		AD5	AH5			LOW
B6	VREF1B6	IO	DIFFIO_TX135p		AE5	AH6			LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO	DIFFIO_TX134n		AC5	AG6			LOW
B6	VREF1B6	IO	DIFFIO_TX134p		AB5	AG5			LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO							LOW
B6	VREF1B6	IO	DIFFIO_TX133n		AA6	AF8			HIGH
B6	VREF1B6	IO	DIFFIO_TX133p		Y6	AF7			HIGH
B6	VREF1B6	IO	DIFFIO_RX133n		AF4	AL4			HIGH
B6	VREF1B6	IO	DIFFIO_RX133p		AE4	AL3			HIGH
B6	VREF2B6	IO	DIFFIO_TX132n		Y9	AF6			HIGH
B6	VREF2B6	IO	DIFFIO_TX132p		W9	AF5			HIGH
B6	VREF2B6	IO	DIFFIO_RX132n		AD4	AK4			HIGH
B6	VREF2B6	IO	DIFFIO_RX132p		AC4	AK3			HIGH
B6	VREF2B6	IO	DIFFIO_TX131n		Y8	AE8			HIGH
B6	VREF2B6	IO	DIFFIO_TX131p		W8	AE7			HIGH
B6	VREF2B6	IO	DIFFIO_RX131n		AG3	AK1			HIGH
B6	VREF2B6	IO	DIFFIO_RX131p		AH3	AK2			HIGH
B6	VREF2B6	IO	DIFFIO_TX130n		AA5	AE6			HIGH
B6	VREF2B6	IO	DIFFIO_TX130p		Y5	AE5			HIGH
B6	VREF2B6	IO	DIFFIO_RX130n		AF3	AJ4			HIGH
B6	VREF2B6	IO	DIFFIO_RX130p		AE3	AJ3			HIGH
B6	VREF2B6	IO	DIFFIO_TX129n		Y7	AD10			HIGH
B6	VREF2B6	IO	DIFFIO_TX129p		W7	AD9			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF2B6	IO	DIFFIO_RX129n		AD3	AJ2			HIGH
B6	VREF2B6	IO	DIFFIO_RX129p		AC3	AJ1			HIGH
B6	VREF2B6	IO	DIFFIO_TX128n		U7	AD8			HIGH
B6	VREF2B6	IO	DIFFIO_TX128p		V7	AD7			HIGH
B6	VREF2B6	IO	DIFFIO_RX128n		AH2	AH4			HIGH
B6	VREF2B6	IO	DIFFIO_RX128p		AG2	AH3			HIGH
B6	VREF2B6	VREF2B6			Y10	AG11			
B6	VREF2B6	IO	DIFFIO_TX127n		W6	AD5			HIGH
B6	VREF2B6	IO	DIFFIO_TX127p		V6	AD6			HIGH
B6	VREF2B6	IO	DIFFIO_RX127n		AE2	AH1			HIGH
B6	VREF2B6	IO	DIFFIO_RX127p		AF2	AH2			HIGH
B6	VREF2B6	IO	DIFFIO_TX126n		U6	AC5			HIGH
B6	VREF2B6	IO	DIFFIO_TX126p		T6	AC6			HIGH
B6	VREF2B6	IO	DIFFIO_RX126n		AD2	AG4			HIGH
B6	VREF2B6	IO	DIFFIO_RX126p		AC2	AG3			HIGH
B6	VREF2B6	IO	DIFFIO_TX125n		W5	AC7			HIGH
B6	VREF2B6	IO	DIFFIO_TX125p		V5	AC8			HIGH
B6	VREF2B6	IO	DIFFIO_RX125n		AF1	AG2			HIGH
B6	VREF2B6	IO	DIFFIO_RX125p		AE1	AF2			HIGH
B6	VREF2B6	IO	DIFFIO_TX124n		T5	AB5			HIGH
B6	VREF2B6	IO	DIFFIO_TX124p		U5	AB6			HIGH
B6	VREF2B6	IO	DIFFIO_RX124n		AD1	AF1			HIGH
B6	VREF2B6	IO	DIFFIO_RX124p		AC1	AE2			HIGH
B6	VREF2B6	IO	DIFFIO_TX123n			AC11			LOW
B6	VREF2B6	IO	DIFFIO_TX123p			AC12			LOW
B6	VREF2B6	IO	DIFFIO_RX123n/RDN6		AB4	AF4			HIGH
B6	VREF2B6	IO	DIFFIO_RX123p/RUP6		AB3	AF3			HIGH
B6	VREF3B6	IO	DIFFIO_TX122n			AC9			LOW
B6	VREF3B6	IO	DIFFIO_TX122p			AC10			LOW
B6	VREF3B6	IO	DIFFIO_RX122n		Y4	AE4			HIGH
B6	VREF3B6	IO	DIFFIO_RX122p		AA4	AE3			HIGH
B6	VREF3B6	IO	DIFFIO_TX121n			AC14			LOW
B6	VREF3B6	IO	DIFFIO_TX121p			AB14			LOW
B6	VREF3B6	IO	DIFFIO_RX121n		W4	AD4			HIGH
B6	VREF3B6	IO	DIFFIO_RX121p		V4	AD3			HIGH
B6	VREF3B6	IO	DIFFIO_TX120n			AB13			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF3B6	IO	DIFFIO_TX120p			AB12			LOW
B6	VREF3B6	IO	DIFFIO_RX120n		AA3	AD2			HIGH
B6	VREF3B6	IO	DIFFIO_RX120p		Y3	AD1			HIGH
B6	VREF3B6	IO	DIFFIO_TX119n			AB10			LOW
B6	VREF3B6	IO	DIFFIO_TX119p			AB11			LOW
B6	VREF3B6	IO	DIFFIO_RX119n		W3	AC4			HIGH
B6	VREF3B6	IO	DIFFIO_RX119p		V3	AC3			HIGH
B6	VREF3B6	IO	DIFFIO_TX118n			AB8			LOW
B6	VREF3B6	IO	DIFFIO_TX118p			AB9			LOW
B6	VREF3B6	IO	DIFFIO_RX118n		AB2	AC2			HIGH
B6	VREF3B6	IO	DIFFIO_RX118p		AA2	AC1			HIGH
B6	VREF3B6	VREF3B6			AA10	AH11			
B6	VREF3B6	IO	DIFFIO_TX117n			AA12			LOW
B6	VREF3B6	IO	DIFFIO_TX117p			AA13			LOW
B6	VREF3B6	IO	DIFFIO_RX117n		Y2	AB4			HIGH
B6	VREF3B6	IO	DIFFIO_RX117p		W2	AB3			HIGH
B6	VREF3B6	IO	DIFFIO_TX116n			AA11			LOW
B6	VREF3B6	IO	DIFFIO_TX116p			AA10			LOW
B6	VREF3B6	IO	DIFFIO_RX116n		AA1	AB1			HIGH
B6	VREF3B6	IO	DIFFIO_RX116p		AB1	AB2			HIGH
B6	VREF3B6	IO	DIFFIO_TX115n			AA9			LOW
B6	VREF3B6	IO	DIFFIO_TX115p			AA8			LOW
B6	VREF3B6	IO	DIFFIO_RX115n		V2	AA4			HIGH
B6	VREF3B6	IO	DIFFIO_RX115p		U2	AA3			HIGH
B6	VREF3B6	IO	DIFFIO_TX114n			AB7			LOW
B6	VREF3B6	IO	DIFFIO_TX114p			AA6			LOW
B6	VREF3B6	IO	DIFFIO_RX114n		V1	AA2			HIGH
B6	VREF3B6	IO	DIFFIO_RX114p		U1	AA1			HIGH
B6	VREF3B6	IO	CLK8n		U4	Y5			
B6	VREF3B6	CLK8p			U3	Y6			
B6	VREF3B6	CLK9n			T3	Y2			
B6	VREF3B6	CLK9p			T4	Y1			
		GNDG_PLL3			V9	Y11			
		VCCG_PLL3			U9	Y12			
		GNDA_PLL3			V8	Y9			
		GND							

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCA_PLL3			U8	W8			
		VCCINT							
		GNDG_PLL4			R9	W11			
		VCCG_PLL4			R10	W12			
		GNDA_PLL4			R8	W9			
		GND							
		VCCA_PLL4			T8	W10			
		VCCINT							
B5	VREF0B5	CLK10p			T1	Y3			
B5	VREF0B5	IO	CLK10n		T2	Y4			
B5	VREF0B5	CLK11p			R3	W5			
B5	VREF0B5	CLK11n			R4	W6			
B5	VREF0B5	IO	DIFFIO_TX113n			Y7			LOW
B5	VREF0B5	IO	DIFFIO_TX113p			W7			LOW
B5	VREF0B5	IO	DIFFIO_RX113n		R1	W1			HIGH
B5	VREF0B5	IO	DIFFIO_RX113p		P1	W2			HIGH
B5	VREF0B5	IO	DIFFIO_TX112n			AA14			LOW
B5	VREF0B5	IO	DIFFIO_TX112p			Y14			LOW
B5	VREF0B5	IO	DIFFIO_RX112n		P2	W4			HIGH
B5	VREF0B5	IO	DIFFIO_RX112p		R2	W3			HIGH
B5	VREF0B5	IO	DIFFIO_TX111n			W13			LOW
B5	VREF0B5	IO	DIFFIO_TX111p			Y13			LOW
B5	VREF0B5	IO	DIFFIO_RX111n		K1	V1			HIGH
B5	VREF0B5	IO	DIFFIO_RX111p		L1	V2			HIGH
B5	VREF0B5	IO	DIFFIO_TX110n			W14			LOW
B5	VREF0B5	IO	DIFFIO_TX110p			V14			LOW
B5	VREF0B5	IO	DIFFIO_RX110n		N2	V3			HIGH
B5	VREF0B5	IO	DIFFIO_RX110p		M2	V4			HIGH
B5	VREF0B5	VREF0B5			L10	M11			
B5	VREF0B5	IO	DIFFIO_TX109n			V7			LOW
B5	VREF0B5	IO	DIFFIO_TX109p			V8			LOW
B5	VREF0B5	IO	DIFFIO_RX109n		L2	U1			HIGH
B5	VREF0B5	IO	DIFFIO_RX109p		K2	U2			HIGH
B5	VREF0B5	IO	DIFFIO_TX108n			V9			LOW
B5	VREF0B5	IO	DIFFIO_TX108p			V10			LOW
B5	VREF0B5	IO	DIFFIO_RX108n		P3	U3			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF0B5	IO	DIFFIO_RX108p		N3	U4			HIGH
B5	VREF0B5	IO	DIFFIO_TX107n			V11			LOW
B5	VREF0B5	IO	DIFFIO_TX107p			V12			LOW
B5	VREF0B5	IO	DIFFIO_RX107n		L3	T2			HIGH
B5	VREF0B5	IO	DIFFIO_RX107p		M3	T1			HIGH
B5	VREF0B5	IO	DIFFIO_TX106n			U13			LOW
B5	VREF0B5	IO	DIFFIO_TX106p			V13			LOW
B5	VREF0B5	IO	DIFFIO_RX106n		P4	T3			HIGH
B5	VREF0B5	IO	DIFFIO_RX106p		N4	T4			HIGH
B5	VREF0B5	IO	DIFFIO_TX105n			U9			LOW
B5	VREF0B5	IO	DIFFIO_TX105p			U10			LOW
B5	VREF0B5	IO	DIFFIO_RX105n		M4	R3			HIGH
B5	VREF0B5	IO	DIFFIO_RX105p		L4	R4			HIGH
B5	VREF1B5	IO	DIFFIO_TX104n			U12			LOW
B5	VREF1B5	IO	DIFFIO_TX104p			U11			LOW
B5	VREF1B5	IO	DIFFIO_RX104n/RDN5		K3	P3			HIGH
B5	VREF1B5	IO	DIFFIO_RX104p/RUP5		K4	P4			HIGH
B5	VREF1B5	IO	DIFFIO_TX103n		R7	V6			HIGH
B5	VREF1B5	IO	DIFFIO_TX103p		T7	V5			HIGH
B5	VREF1B5	IO	DIFFIO_RX103n		J1	R2			HIGH
B5	VREF1B5	IO	DIFFIO_RX103p		H1	P1			HIGH
B5	VREF1B5	IO	DIFFIO_TX102n		P8	U8			HIGH
B5	VREF1B5	IO	DIFFIO_TX102p		N8	U7			HIGH
B5	VREF1B5	IO	DIFFIO_RX102n		G1	P2			HIGH
B5	VREF1B5	IO	DIFFIO_RX102p		F1	N2			HIGH
B5	VREF1B5	IO	DIFFIO_TX101n		R6	U6			HIGH
B5	VREF1B5	IO	DIFFIO_TX101p		P6	U5			HIGH
B5	VREF1B5	IO	DIFFIO_RX101n		H2	N4			HIGH
B5	VREF1B5	IO	DIFFIO_RX101p		J2	N3			HIGH
B5	VREF1B5	IO	DIFFIO_TX100n		P9	T5			HIGH
B5	VREF1B5	IO	DIFFIO_TX100p		N9	T6			HIGH
B5	VREF1B5	IO	DIFFIO_RX100n		G2	M1			HIGH
B5	VREF1B5	IO	DIFFIO_RX100p		F2	M2			HIGH
B5	VREF1B5	VREF1B5			M10	N11			
B5	VREF1B5	IO	DIFFIO_TX99n		P7	T7			HIGH
B5	VREF1B5	IO	DIFFIO_TX99p		N7	T8			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF1B5	IO	DIFFIO_RX99n		J3	M3			HIGH
B5	VREF1B5	IO	DIFFIO_RX99p		H3	M4			HIGH
B5	VREF1B5	IO	DIFFIO_TX98n		N6	T9			HIGH
B5	VREF1B5	IO	DIFFIO_TX98p		M6	T10			HIGH
B5	VREF1B5	IO	DIFFIO_RX98n		G3	L1			HIGH
B5	VREF1B5	IO	DIFFIO_RX98p		F3	L2			HIGH
B5	VREF1B5	IO	DIFFIO_TX97n		R5	R5			HIGH
B5	VREF1B5	IO	DIFFIO_TX97p		P5	R6			HIGH
B5	VREF1B5	IO	DIFFIO_RX97n		J4	L3			HIGH
B5	VREF1B5	IO	DIFFIO_RX97p		H4	L4			HIGH
B5	VREF1B5	IO	DIFFIO_TX96n		M5	R8			HIGH
B5	VREF1B5	IO	DIFFIO_TX96p		N5	R7			HIGH
B5	VREF1B5	IO	DIFFIO_RX96n		G4	K2			HIGH
B5	VREF1B5	IO	DIFFIO_RX96p		F4	K1			HIGH
B5	VREF1B5	IO	DIFFIO_TX95n		M8	P5			HIGH
B5	VREF1B5	IO	DIFFIO_TX95p		L8	P6			HIGH
B5	VREF1B5	IO	DIFFIO_RX95n		E2	K3			HIGH
B5	VREF1B5	IO	DIFFIO_RX95p		D2	K4			HIGH
B5	VREF2B5	IO	DIFFIO_TX94n		M7	P7			HIGH
B5	VREF2B5	IO	DIFFIO_TX94p		L7	P8			HIGH
B5	VREF2B5	IO	DIFFIO_RX94n		E3	J3			HIGH
B5	VREF2B5	IO	DIFFIO_RX94p		D3	J4			HIGH
B5	VREF2B5	IO	DIFFIO_TX93n		L5	N5			LOW
B5	VREF2B5	IO	DIFFIO_TX93p		K5	N6			LOW
B5	VREF2B5	IO							LOW
B5	VREF2B5	IO							LOW
B5	VREF2B5	IO	DIFFIO_TX92n		H5	N8			LOW
B5	VREF2B5	IO	DIFFIO_TX92p		J5	N7			LOW
B5	VREF2B5	IO							LOW
B5	VREF2B5	IO							LOW
B5	VREF2B5	IO	DIFFIO_TX91n		F5	M6			LOW
B5	VREF2B5	IO	DIFFIO_TX91p		G5	M5			LOW
B5	VREF2B5	IO							LOW
B5	VREF2B5	IO							LOW
B5	VREF2B5	IO	DIFFIO_TX90n		L6	L5			LOW
B5	VREF2B5	IO	DIFFIO_TX90p		K6	L6			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF2B5	IO							LOW
B5	VREF2B5	IO							LOW
B5	VREF2B5	VREF2B5			N10	P11			
B5	VREF2B5	IO	DIFFIO_TX89n		J6	M7			LOW
B5	VREF2B5	IO	DIFFIO_TX89p		H6	M8			LOW
B5	VREF2B5	IO	DIFFIO_RX89n			H2			LOW
B5	VREF2B5	IO	DIFFIO_RX89p			H1			LOW
B5	VREF2B5	IO	DIFFIO_TX88n		G6	K5			LOW
B5	VREF2B5	IO	DIFFIO_TX88p		F6	K6			LOW
B5	VREF2B5	IO	DIFFIO_RX88n			G2			LOW
B5	VREF2B5	IO	DIFFIO_RX88p			G1			LOW
B5	VREF2B5	IO	DIFFIO_TX87n		K8	L8			LOW
B5	VREF2B5	IO	DIFFIO_TX87p		J8	L7			LOW
B5	VREF2B5	IO	DIFFIO_RX87n			F1			LOW
B5	VREF2B5	IO	DIFFIO_RX87p			F2			LOW
B5	VREF2B5	IO	DIFFIO_TX86n		K7	K7			LOW
B5	VREF2B5	IO	DIFFIO_TX86p		J7	K8			LOW
B5	VREF2B5	IO	DIFFIO_RX86n			E1			LOW
B5	VREF2B5	IO	DIFFIO_RX86p			E2			LOW
B5	VREF2B5	IO	DIFFIO_TX85n		H7	J7			LOW
B5	VREF2B5	IO	DIFFIO_TX85p		G7	J8			LOW
B5	VREF2B5	IO	DIFFIO_RX85n			D1			LOW
B5	VREF2B5	IO	DIFFIO_RX85p			D2			LOW
B5	VREF3B5	IO	DIFFIO_TX84n		G8	M9			LOW
B5	VREF3B5	IO	DIFFIO_TX84p		H8	M10			LOW
B5	VREF3B5	IO	DIFFIO_RX84n			H3			LOW
B5	VREF3B5	IO	DIFFIO_RX84p			H4			LOW
B5	VREF3B5	IO	DIFFIO_TX83n			R10			LOW
B5	VREF3B5	IO	DIFFIO_TX83p			R9			LOW
B5	VREF3B5	IO	DIFFIO_RX83n			G4			LOW
B5	VREF3B5	IO	DIFFIO_RX83p			G3			LOW
B5	VREF3B5	IO	DIFFIO_TX82n			P10			LOW
B5	VREF3B5	IO	DIFFIO_TX82p			P9			LOW
B5	VREF3B5	IO	DIFFIO_RX82n			F3			LOW
B5	VREF3B5	IO	DIFFIO_RX82p			F4			LOW
B5	VREF3B5	IO	DIFFIO_TX81n			N9			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF3B5	IO	DIFFIO_TX81p			N10			LOW
B5	VREF3B5	IO	DIFFIO_RX81n			E3			LOW
B5	VREF3B5	IO	DIFFIO_RX81p			E4			LOW
B5	VREF3B5	IO	DIFFIO_TX80n			T13			LOW
B5	VREF3B5	IO	DIFFIO_TX80p			U14			LOW
B5	VREF3B5	IO	DIFFIO_RX80n			C2			LOW
B5	VREF3B5	IO	DIFFIO_RX80p			D3			LOW
B5	VREF3B5	VREF3B5			P10	R11			
B5	VREF3B5	IO	DIFFIO_TX79n			T11			LOW
B5	VREF3B5	IO	DIFFIO_TX79p			T12			LOW
B5	VREF3B5	IO	DIFFIO_RX79n			J5			LOW
B5	VREF3B5	IO	DIFFIO_RX79p			J6			LOW
B5	VREF3B5	IO	DIFFIO_TX78n			R13			LOW
B5	VREF3B5	IO	DIFFIO_TX78p			R12			LOW
B5	VREF3B5	IO	DIFFIO_RX78n			H6			LOW
B5	VREF3B5	IO	DIFFIO_RX78p			H5			LOW
B5	VREF3B5	IO	DIFFIO_TX77n			R14			LOW
B5	VREF3B5	IO	DIFFIO_TX77p			T14			LOW
B5	VREF3B5	IO	DIFFIO_RX77n			G5			LOW
B5	VREF3B5	IO	DIFFIO_RX77p			G6			LOW
B5	VREF3B5	IO	DIFFIO_TX76n			N12			LOW
B5	VREF3B5	IO	DIFFIO_TX76p			P12			LOW
B5	VREF3B5	IO	DIFFIO_RX76n			F5			LOW
B5	VREF3B5	IO	DIFFIO_RX76p			F6			LOW
B5	VREF3B5	IO				P13			
B5	VREF3B5	IO				P14			
B5	VREF3B5	FPLL10CLKn			D1	J1			
B5	VREF3B5	FPLL10CLKp			E1	J2			
		GNDG_PLL10			K9	L9			
		VCCG_PLL10			J9	L10			
		GNDA_PLL10			M9	K9			
		GND							
		VCCA_PLL10			L9	J9			
		VCCINT							
B4	VREF0B4	IO							
B4	VREF0B4	IO				B3			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF0B4	IO				D4			
B4	VREF0B4	IO			C2	G8			
B4	VREF0B4	IO				G7			
B4	VREF0B4	IO				E5			
B4	VREF0B4	IO				C4			
B4	VREF0B4	IO				G9			
B4	VREF0B4	IO				H9			
B4	VREF0B4	IO			E5	E6			
B4	VREF0B4	IO	DQ0T0		C4	C6	DQ0T0	DQ0T0	
B4	VREF0B4	IO				J10			
B4	VREF0B4	IO	DQ0T1		C5	B6	DQ0T1	DQ0T1	
B4	VREF0B4	IO			F8	D6			
B4	VREF0B4	IO	DQ0T2		D5	C7	DQ0T2	DQ0T2	
B4	VREF0B4	IO			D4	F8			
B4	VREF0B4	IO	DQS0T		B4	B7			
B4	VREF0B4	IO			E4	F7			
B4	VREF0B4	VREF0B4			K10	L11			
B4	VREF0B4	IO	DQ0T3		B5	A7	DQ0T3	DQ0T3	
B4	VREF0B4	IO				D7			
B4	VREF0B4	IO	DQ0T4		B3	C8	DQ0T4	DQ0T4	
B4	VREF0B4	IO			F7	E7			
B4	VREF0B4	IO	DQ0T5		C3	A6	DQ0T5	DQ0T5	
B4	VREF0B4	IO			H9	D5			
B4	VREF0B4	IO	DQ0T6		A5	A8	DQ0T6	DQ0T6	
B4	VREF0B4	IO				F9			
B4	VREF0B4	IO	DQ0T7		A4	B8	DQ0T7	DQ0T7	
B4	VREF0B4	IO			G9	C5			
B4	VREF0B4	IO				K11			
B4	VREF0B4	IO				J11			
B4	VREF1B4	IO				G10			
B4	VREF1B4	IO				B5			
B4	VREF1B4	IO				B4			
B4	VREF1B4	IO				J12			
B4	VREF1B4	IO				K12			
B4	VREF1B4	IO	DQ1T0		E6	C9	DQ0T8	DQ0T8	
B4	VREF1B4	IO				F10			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF1B4	IO	DQ1T1		C7	B9	DQ0T9	DQ0T9	
B4	VREF1B4	IO			E7	E8			
B4	VREF1B4	IO	DQ1T2		D7	A9	DQ0T10	DQ0T10	
B4	VREF1B4	IO				H11			
B4	VREF1B4	IO	DQS1T		C6	B10	DQS0T		
B4	VREF1B4	IO			F9	G11			
B4	VREF1B4	IO	DQ1T3		A6	C11	DQ0T11	DQ0T11	
B4	VREF1B4	IO			H10	A4			
B4	VREF1B4	IO	DQ1T4		B6	A10	DQ0T12	DQ0T12	
B4	VREF1B4	IO				K13			
B4	VREF1B4	IO	DQ1T5		D6	C10	DQ0T13	DQ0T13	
B4	VREF1B4	VREF1B4			K11	L12			
B4	VREF1B4	IO			E9	A5			
B4	VREF1B4	IO	DQ1T6		A7	A11	DQ0T14	DQ0T14	
B4	VREF1B4	IO			G10	J13			
B4	VREF1B4	IO	DQ1T7		B7	B11	DQ0T15	DQ0T15	
B4	VREF1B4	IO			J10	M12			
B4	VREF1B4	IO				H12			
B4	VREF1B4	IO				F11			
B4	VREF1B4	IO				H13			
B4	VREF1B4	IO				D8			
B4	VREF1B4	IO				E10			
B4	VREF1B4	IO				M13			
B4	VREF1B4	IO				E9			
B4	VREF2B4	IO	DQ2T0		B8	A12	DQ1T0	DQ0T16	
B4	VREF2B4	IO				D10			
B4	VREF2B4	IO	DQ2T1		D9	D12	DQ1T1	DQ0T17	
B4	VREF2B4	IO			G11	J14			
B4	VREF2B4	IO	DQ2T2		E8	E12	DQ1T2	DQ0T18	
B4	VREF2B4	IO				D9			
B4	VREF2B4	IO	DQS2T		C8	C12		DQS0T	
B4	VREF2B4	IO			G12	G13			
B4	VREF2B4	IO	DQ2T3		C9	E13	DQ1T3	DQ0T19	
B4	VREF2B4	IO			H11	G12			
B4	VREF2B4	IO	DQ2T4		D8	B12	DQ1T4	DQ0T20	
B4	VREF2B4	IO				K14			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF2B4	IO	DQ2T5		A9	B13	DQ1T5	DQ0T21	
B4	VREF2B4	IO				F13			
B4	VREF2B4	IO	DQ2T6		B9	C13	DQ1T6	DQ0T22	
B4	VREF2B4	IO			J11	F12			
B4	VREF2B4	IO	DQ2T7		A8	D13	DQ1T7	DQ0T23	
B4	VREF2B4	IO				N13			
B4	VREF2B4	VREF2B4			K12	L13			
B4	VREF2B4	IO	FCLK6		F10	D11			
B4	VREF2B4	IO	FCLK7		F11	G14			
B4	VREF2B4	IO				E11			
B4	VREF2B4	IO				H14			
B4	VREF2B4	IO				M14			
B4	VREF2B4	IO				N14			
B4	VREF2B4	IO				F14			
B4	VREF2B4	IO	DQ3T0		B10	C14	DQ1T8	DQ0T24	
B4	VREF2B4	IO				J15			
B4	VREF2B4	IO	DQ3T1		D10	D14	DQ1T9	DQ0T25	
B4	VREF2B4	IO			L11	K15			
B4	VREF2B4	IO	DQ3T2		E10	E14	DQ1T10	DQ0T26	
B4	VREF3B4	IO			H12	H15			
B4	VREF3B4	IO	DQS3T		C10	C15	DQS1T		
B4	VREF3B4	IO				M15			
B4	VREF3B4	IO	DQ3T3		D11	A14	DQ1T11	DQ0T27	
B4	VREF3B4	IO			J12	N15			
B4	VREF3B4	IO	DQ3T4		E11	B14	DQ1T12	DQ0T28	
B4	VREF3B4	IO			G13	G15			
B4	VREF3B4	IO	DQ3T5		B11	B15	DQ1T13	DQ0T29	
B4	VREF3B4	IO				P15			
B4	VREF3B4	IO	DQ3T6		C11	E15	DQ1T14	DQ0T30	
B4	VREF3B4	IO	DEV_OE		F12	P16			
B4	VREF3B4	IO	DQ3T7		A10	D15	DQ1T15	DQ0T31	
B4	VREF3B4	IO	RUP4		F13	F15			
B4	VREF3B4	IO	RDN4		E14	E16			
B4	VREF3B4	IO				L16			
B4	VREF3B4	IO				J16			
B4	VREF3B4	IO				M16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF3B4	IO				K16			
B4	VREF3B4	VREF3B4			K13	L14			
B4	VREF3B4	IO				G16			
B4	VREF3B4	IO			L12	H16			
B4	VREF3B4	IO	DQ4T0		D12	A16			
B4	VREF3B4	IO		nWS	F14	F16			
B4	VREF3B4	IO	DQ4T1		E12	D16			
B4	VREF3B4	IO				N16			
B4	VREF3B4	IO	DQ4T2		A12	A17			
B4	VREF3B4	IO			H13	F17			
B4	VREF3B4	IO	DQS4T		C12	C16			
B4	VREF3B4	IO		DATA0	E15	M17			
B4	VREF3B4	IO	DQ4T3		B12	B16			
B4	VREF3B4	IO				P17			
B4	VREF4B4	IO	DQ4T4		C13	B17			
B4	VREF4B4	IO			G14	H17			
B4	VREF4B4	IO	DQ4T5		D13	D17			
B4	VREF4B4	IO		DATA1	C16	J17			
B4	VREF4B4	IO	DQ4T6		E13	E17			
B4	VREF4B4	IO				K17			
B4	VREF4B4	IO	DQ4T7		B13	C17			
B4	VREF4B4	IO			J13	C18			
B4	VREF4B4	IO				G17			
B4	VREF4B4	IO				P18			
B4	VREF4B4	IO				L17			
B4	VREF4B4	IO				N17			
B4	VREF4B4	IO				D18			
B4	VREF4B4	IO				F18			
B4	VREF4B4	IO			L14	E18			
B4	VREF4B4	IO				L18			
B4	VREF4B4	IO				N18			
B4	VREF4B4	IO				M18			
B4	VREF4B4	VREF4B4			K14	L15			
B4	VREF4B4	IO				G18			
B4	VREF4B4	IO				H18			
B4	VREF4B4	IO			L16	J18			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF4B4	IO		DATA2	F15	K18			
B4	VREF4B4	IO				P19			
B4	VREF4B4	IO				N19			
B4	VREF4B4	TMS		TMS	D16	F19			
B4	VREF4B4	TRST		TRST	G15	H19			
B4	VREF4B4	TCK		TCK	F16	E20			
B4	VREF4B4	IO		DATA3	G17	P21			
B4	VREF4B4	IO				P20			
B4	VREF4B4	IO				N20			
B4	VREF4B4	TDI		TDI	E16	F20			
B4	VREF4B4	TDO		TDO	G16	G20			
B4	VREF4B4	IO	CLK12n		B14	A18			
B4	VREF4B4	CLK12p			A14	B18			
B4	VREF4B4	IO	CLK13n/PLL11_OUT		D14	C19			
B4	VREF4B4	CLK13p			C14	D19			
		VCCINT							
		VCCA_PLL11			J14	K19			
		GND							
		GNDA_PLL11			H14	J19			
		VCCG_PLL11			H15	L19			
		GNDG_PLL11			J15	M19			
		TEMPDIODEp			E17	F21			
		TEMPDIODEn			F17	H21			
		VCCINT							
		VCCA_PLL5			J17	L21			
		GND							
		GNDA_PLL5			H16	M21			
		VCCG_PLL5			K15	L20			
		GNDG_PLL5			K17	M20			
B9		VCC_PLL5_OUTA			L18	J20			
B9		VCC_PLL5_OUTA							
B10		VCC_PLL5_OUTB			J18	K21			
B10		VCC_PLL5_OUTB							
B9	VREF0B3	IO	PLL5_OUT0p		B16	C21			
B9	VREF0B3	IO	PLL5_OUT0n		A16	D21			
B9	VREF0B3	IO	PLL5_OUT1p		B15	C20			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B9	VREF0B3	IO	PLL5_OUT1n		A15	D20			
B9	VREF0B3	IO	PLL5_FBp		D15	B19			
B9	VREF0B3	IO	PLL5_FBn		C15	A19			
B10	VREF0B3	IO	PLL5_OUT2p		D17	B21			
B10	VREF0B3	IO	PLL5_OUT2n		C17	A21			
B10	VREF0B3	IO	PLL5_OUT3p		B17	A20			
B10	VREF0B3	IO	PLL5_OUT3n		A17	B20			
B3	VREF0B3	nSTATUS		nSTATUS	E18	N21			
B3	VREF0B3	nCONFIG		nCONFIG	F19	L22			
B3	VREF0B3	DCLK		DCLK	F18	G21			
B3	VREF0B3	CONF_DONE		CONF_DONE	G18	H22			
B3	VREF0B3	CLK14p			A18	B22			
B3	VREF0B3	IO	CLK14n		B18	A22			
B3	VREF0B3	CLK15p			C18	D22			
B3	VREF0B3	IO	CLK15n		D18	C22			
B3	VREF0B3	VREF0B3			K18	L25			
B3	VREF0B3	IO				E21			
B3	VREF0B3	IO				G22			
B3	VREF0B3	IO				J22			
B3	VREF0B3	IO				N22			
B3	VREF0B3	IO				M22			
B3	VREF0B3	IO				P22			
B3	VREF0B3	IO				E22			
B3	VREF0B3	IO				G23			
B3	VREF0B3	IO			L19	F22			
B3	VREF0B3	IO		DATA4	G19	L23			
B3	VREF0B3	IO				N23			
B3	VREF0B3	IO	DQ5T0		B19	B23			
B3	VREF0B3	IO			J19	H23			
B3	VREF0B3	IO	DQ5T1		C19	E23			
B3	VREF0B3	IO		DATA5	F20	J23			
B3	VREF0B3	IO	DQ5T2		D19	D23			
B3	VREF0B3	IO				K23			
B3	VREF0B3	IO	DQS5T		C20	C23			
B3	VREF1B3	IO			H19	F23			
B3	VREF1B3	IO	DQ5T3		E19	A23			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF1B3	IO		DATA6	F21	E24			
B3	VREF1B3	IO	DQ5T4		A20	A24			
B3	VREF1B3	IO				M23			
B3	VREF1B3	IO	DQ5T5		B20	B24			
B3	VREF1B3	IO			H20	F24			
B3	VREF1B3	IO	DQ5T6		D20	C24			
B3	VREF1B3	IO				G24			
B3	VREF1B3	IO	DQ5T7		E20	D24			
B3	VREF1B3	IO			J20	K24			
B3	VREF1B3	IO				N24			
B3	VREF1B3	VREF1B3			K19	L26			
B3	VREF1B3	IO				H24			
B3	VREF1B3	IO				F25			
B3	VREF1B3	IO				J24			
B3	VREF1B3	IO				L24			
B3	VREF1B3	IO	RUP3		F22	P23			
B3	VREF1B3	IO	RDN3		F24	M24			
B3	VREF1B3	IO	DQ6T0		B21	B25	DQ2T0	DQ1T0	
B3	VREF1B3	IO				G25			
B3	VREF1B3	IO	DQ6T1		C21	E25	DQ2T1	DQ1T1	
B3	VREF1B3	IO		DATA7	G20	P25			
B3	VREF1B3	IO	DQ6T2		A22	D25	DQ2T2	DQ1T2	
B3	VREF1B3	IO				P24			
B3	VREF1B3	IO	DQS6T		C22	C25	DQS2T		
B3	VREF1B3	IO				H25			
B3	VREF1B3	IO	DQ6T3		D21	A26	DQ2T3	DQ1T3	
B3	VREF1B3	IO		CLKUSR	F23	J25			
B3	VREF1B3	IO	DQ6T4		E21	B26	DQ2T4	DQ1T4	
B3	VREF1B3	IO				N25			
B3	VREF2B3	IO	DQ6T5		B22	C26	DQ2T5	DQ1T5	
B3	VREF2B3	IO				F26			
B3	VREF2B3	IO	DQ6T6		D22	D26	DQ2T6	DQ1T6	
B3	VREF2B3	IO				G27			
B3	VREF2B3	IO	DQ6T7		E22	E26	DQ2T7	DQ1T7	
B3	VREF2B3	IO				K25			
B3	VREF2B3	IO	FCLK0		E23	G26			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF2B3	IO	FCLK1		E25	D29			
B3	VREF2B3	IO				H26			
B3	VREF2B3	IO				D30			
B3	VREF2B3	IO				M25			
B3	VREF2B3	IO				N26			
B3	VREF2B3	VREF2B3			K20	L27			
B3	VREF2B3	IO				F27			
B3	VREF2B3	IO	DQ7T0		A23	B27	DQ2T8	DQ1T8	
B3	VREF2B3	IO				E29			
B3	VREF2B3	IO	DQ7T1		B23	C27	DQ2T9	DQ1T9	
B3	VREF2B3	IO			L21	M26			
B3	VREF2B3	IO	DQ7T2		A24	D27	DQ2T10	DQ1T10	
B3	VREF2B3	IO				F28			
B3	VREF2B3	IO	DQS7T		C24	C28		DQS1T	
B3	VREF2B3	IO			H21	F29			
B3	VREF2B3	IO	DQ7T3		C23	E27	DQ2T11	DQ1T11	
B3	VREF2B3	IO			J21	N27			
B3	VREF2B3	IO	DQ7T4		D24	B28	DQ2T12	DQ1T12	
B3	VREF2B3	IO				D31			
B3	VREF2B3	IO	DQ7T5		B24	A28	DQ2T13	DQ1T13	
B3	VREF2B3	IO				J26			
B3	VREF2B3	IO	DQ7T6		D23	D28	DQ2T14	DQ1T14	
B3	VREF2B3	IO				K26			
B3	VREF2B3	IO	DQ7T7		E24	E28	DQ2T15	DQ1T15	
B3	VREF3B3	IO				H27			
B3	VREF3B3	IO				E30			
B3	VREF3B3	IO				A35			
B3	VREF3B3	IO				F30			
B3	VREF3B3	IO				M27			
B3	VREF3B3	IO				N28			
B3	VREF3B3	IO				G28			
B3	VREF3B3	IO			G21	D32			
B3	VREF3B3	IO	DQ8T0		A25	A29	DQ3T0	DQ1T16	
B3	VREF3B3	IO			J22	J27			
B3	VREF3B3	IO	DQ8T1		C25	B29	DQ3T1	DQ1T17	
B3	VREF3B3	IO				M28			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF3B3	VREF3B3			K21	L28			
B3	VREF3B3	IO	DQ8T2		B25	C29	DQ3T2	DQ1T18	
B3	VREF3B3	IO			H22	H28			
B3	VREF3B3	IO	DQS8T		C26	B30	DQS3T		
B3	VREF3B3	IO				E31			
B3	VREF3B3	IO	DQ8T3		D25	C30	DQ3T3	DQ1T19	
B3	VREF3B3	IO				K27			
B3	VREF3B3	IO	DQ8T4		A26	A30	DQ3T4	DQ1T20	
B3	VREF3B3	IO				G29			
B3	VREF3B3	IO	DQ8T5		B26	A31	DQ3T5	DQ1T21	
B3	VREF3B3	IO			G22	D33			
B3	VREF3B3	IO	DQ8T6		E26	B31	DQ3T6	DQ1T22	
B3	VREF3B3	IO				H29			
B3		GND							
B3		GND							
B3		GND			D28	E32			
B3	VREF3B3	IO	DQ8T7		D26	C31	DQ3T7	DQ1T23	
B3	VREF3B3	IO				G30			
B3	VREF3B3	IO				J28			
B3	VREF3B3	IO				B35			
B3	VREF3B3	IO				C35			
B3	VREF3B3	IO				K28			
B3	VREF4B3	IO				F31			
B3	VREF4B3	IO				B36			
B3	VREF4B3	IO			F25	D34			
B3	VREF4B3	IO	DQ9T0		B27	A32	DQ3T8	DQ1T24	
B3	VREF4B3	IO				J29			
B3	VREF4B3	IO	DQ9T1		C27	C32	DQ3T9	DQ1T25	
B3	VREF4B3	IO			G23	A36			
B3	VREF4B3	IO	DQ9T2		A27	B32	DQ3T10	DQ1T26	
B3	VREF4B3	IO			C30	F32			
B3	VREF4B3	IO	DQS9T		B28	B33			
B3	VREF4B3	IO				K29			
B3	VREF4B3	IO	DQ9T3		D27	A34	DQ3T11	DQ1T27	
B3	VREF4B3	VREF4B3			K22	L29			
B3	VREF4B3	IO				E33			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF4B3	IO	DQ9T4		A28	A33	DQ3T12	DQ1T28	
B3	VREF4B3	IO			E27	B37			
B3	VREF4B3	IO	DQ9T5		C28	C33	DQ3T13	DQ1T29	
B3	VREF4B3	IO				F33			
B3	VREF4B3	IO	DQ9T6		C29	C34	DQ3T14	DQ1T30	
B3	VREF4B3	IO				G31			
B3	VREF4B3	IO	DQ9T7		B29	B34	DQ3T15	DQ1T31	
B3	VREF4B3	IO			H23	D35			
B3	VREF4B3	IO				H31			
B3	VREF4B3	IO				J30			
B3	VREF4B3	IO				G33			
B3	VREF4B3	IO				C36			
B3	VREF4B3	IO				E34			
B3	VREF4B3	IO			E28	G32			
B3	VREF4B3	IO				D36			
B3	VREF4B3	IO				E35			
B3	VREF4B3	IO							
		VCCIO2			C31	C39			
		VCCIO2			N31	R39			
		VCCIO2			T23	W35			
		VCCIO2				V25			
		VCCIO2				H33			
		VCCIO1			U20	AA25			
		VCCIO1			W31	Y32			
		VCCIO1			AJ31	AE39			
		VCCIO1				AU39			
		VCCIO1				AM33			
		VCCIO8			AL29	AW37			
		VCCIO8			AL19	AW25			
		VCCIO8			Y17	AR21			
		VCCIO8				AE22			
		VCCIO8				AM30			
		VCCIO7			AC16	AE19			
		VCCIO7			AL13	AM20			
		VCCIO7			AL3	AW15			
		VCCIO7				AW3			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCIO7				AM10			
		VCCIO6			AJ1	AU1			
		VCCIO6			W1	AM7			
		VCCIO6			U12	AE1			
		VCCIO6				AA5			
		VCCIO6				AB15			
		VCCIO5			T9	W15			
		VCCIO5			N1	Y8			
		VCCIO5			C1	R1			
		VCCIO5				H7			
		VCCIO5				C1			
		VCCIO4			A3	A3			
		VCCIO4			A13	A15			
		VCCIO4			J16	E19			
		VCCIO4				R18			
		VCCIO4				H10			
		VCCIO3			M17	H20			
		VCCIO3			A19	R21			
		VCCIO3			A29	A25			
		VCCIO3				A37			
		VCCIO3				H30			
		VCCINT			AA12	AA16			
		VCCINT			AA14	AA18			
		VCCINT			AA20	AA22			
		VCCINT			L13	AA24			
		VCCINT			L20	AB17			
		VCCINT			M11	AB19			
		VCCINT			M13	AB21			
		VCCINT			M15	AB23			
		VCCINT			M19	AB25			
		VCCINT			M21	AC16			
		VCCINT			N12	AC18			
		VCCINT			N14	AC20			
		VCCINT			N16	AC22			
		VCCINT			N18	AC24			
		VCCINT			N20	AD15			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT			P11	AD17			
		VCCINT			P13	AD19			
		VCCINT			P14	AD21			
		VCCINT			P15	AD23			
		VCCINT			P17	AD25			
		VCCINT			P19	AE16			
		VCCINT			P21	AE18			
		VCCINT			R12	AE20			
		VCCINT			R13	AE24			
		VCCINT			R14	R16			
		VCCINT			R18	R20			
		VCCINT			R19	R22			
		VCCINT			R20	R24			
		VCCINT			T11	T15			
		VCCINT			T13	T17			
		VCCINT			T19	T19			
		VCCINT			T21	T21			
		VCCINT			U10	T23			
		VCCINT			U14	T25			
		VCCINT			U18	U16			
		VCCINT			U22	U18			
		VCCINT			V11	U20			
		VCCINT			V13	U22			
		VCCINT			V15	U24			
		VCCINT			V17	V15			
		VCCINT			V19	V17			
		VCCINT			V21	V19			
		VCCINT			W12	V21			
		VCCINT			W14	V23			
		VCCINT			W16	W16			
		VCCINT			W18	W18			
		VCCINT			W20	W22			
		VCCINT			Y11	W24			
		VCCINT			Y13	Y15			
		VCCINT			Y15	Y17			
		VCCINT			Y19	Y23			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT			Y21	Y25			
		GND			A1	A13			
		GND			A11	A2			
		GND			A2	A27			
		GND			A21	A38			
		GND			A30	AA15			
		GND			A31	AA17			
		GND			AA17	AA23			
		GND			AA18	AA7			
		GND			AB16	AB16			
		GND			AD18	AB18			
		GND			AK1	AB20			
		GND			AK2	AB22			
		GND			AK30	AB24			
		GND			AK31	AC15			
		GND			AL1	AC17			
		GND			AL11	AC19			
		GND			AL2	AC21			
		GND			AL21	AC23			
		GND			AL30	AC25			
		GND			AL31	AD16			
		GND			B1	AD18			
		GND			B2	AD20			
		GND			B30	AD22			
		GND			B31	AD24			
		GND			H17	AE15			
		GND			H18	AE17			
		GND			K16	AE21			
		GND			L15	AE23			
		GND			L17	AE25			
		GND			M1	AG1			
		GND			M12	AG39			
		GND			M14	AK10			
		GND			M16	AK20			
		GND			M18	AK22			
		GND			M20	AK30			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			M31	AL21			
		GND			N11	AM32			
		GND			N13	AM8			
		GND			N15	AN21			
		GND			N17	AU3			
		GND			N19	AU37			
		GND			N21	AV1			
		GND			P12	AV2			
		GND			P16	AV38			
		GND			P18	AV39			
		GND			P20	AW13			
		GND			R11	AW2			
		GND			R15	AW27			
		GND			R17	AW38			
		GND			R21	B1			
		GND			T10	B2			
		GND			T12	B38			
		GND			T14	B39			
		GND			T18	C3			
		GND			T20	C37			
		GND			T22	G19			
		GND			U11	H32			
		GND			U13	H8			
		GND			U15	J21			
		GND			U17	K10			
		GND			U19	K20			
		GND			U21	K22			
		GND			V12	K30			
		GND			V14	N1			
		GND			V16	N39			
		GND			V18	R15			
		GND			V20	R17			
		GND			W11	R19			
		GND			W13	R23			
		GND			W15	R25			
		GND			W17	T16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B956	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			W19	T18			
		GND			W21	T20			
		GND			Y1	T22			
		GND			Y12	T24			
		GND			Y14	U15			
		GND			Y16	U17			
		GND			Y18	U19			
		GND			Y20	U21			
		GND			Y31	U23			
		GND				U25			
		GND				V16			
		GND				V18			
		GND				V20			
		GND				V22			
		GND				V24			
		GND				W17			
		GND				W23			
		GND				W25			
		GND				W33			
		GND				Y10			
		GND				Y16			
		GND				Y18			
		GND				Y22			
		GND				Y24			
		GND				Y30			
Note to Pin-List:									

1) The wire bond and flip-chip packages will have different data rates for the high speed differential I/O channels. The following table shows the data rates as supported for each package.

Package	Package Type	High Speed Differential I/O Channel Performance (DIFFIO Speed)		Units
		High	Low	
B956	flip chip	840	462	Mbps
F1508	flip chip	840	462	Mbps

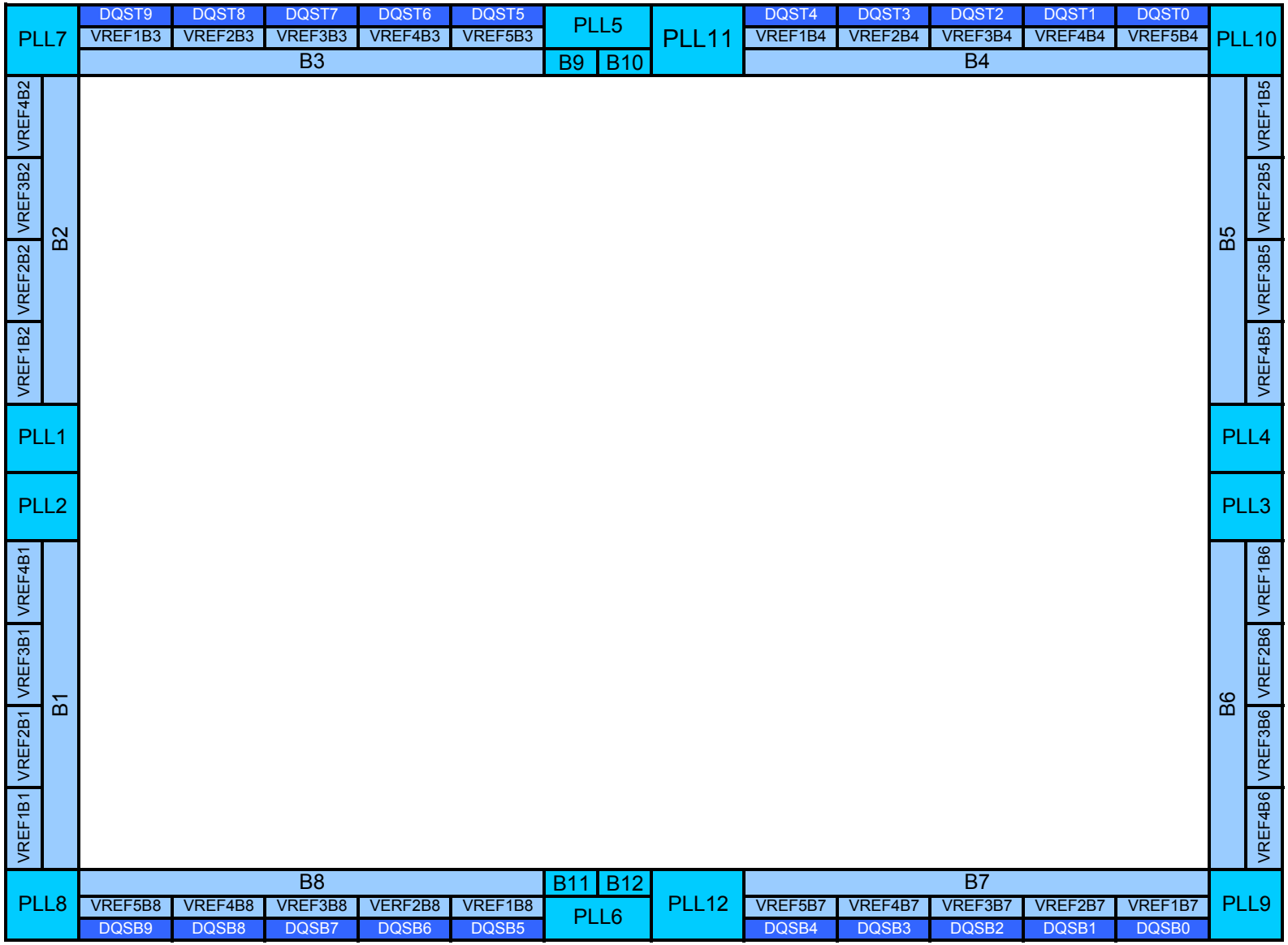
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..8]	Input	Input reference voltage for bank 1. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, designers should connect them to either VCC or Gnd.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1..12]	Power	Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1..12]	Ground	Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA.
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
Clock and PLL Pins		

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Dedicated fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins.
FPLL[10..7]CLKp	Input	Dedicated global clock inputs for fast PLLs (PLLs 7 through 10).
FPLL[10..7]CLKn	Input	Dedicated negative terminal associated with FPLL[10..7]CLKp pins.
CLK[15..0]p	Input	Dedicated global clock inputs 0 to 15.
CLK[15..0]n	Input	Dedicated negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	Output	Dedicated external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6).
PLL6_OUT[3..0]n	Output	Dedicated negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL5_OUT[3..0]p	Output	Dedicated external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5).
PLL5_OUT[3..0]n	Output	Dedicated negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
Optional/Dual-Purpose Pins		
DIFFIO_RX[0..151]p	I/O, Input	Dual-purpose high speed differential I/O receiver channels 0 to 151. If not used, these pins are regular I/O pins.
DIFFIO_RX[0..151]n	I/O, Input	This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel.
DIFFIO_TX[0..151]p	I/O, Output	Dual-purpose high speed differential I/O transmitter channels 114 to 151. If not used, these pins are regular I/O pins.
DIFFIO_TX[0..151]n	I/O, Output	This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel.
CLK6n, PLL12_OUT	I/O, Input (CLK6n), Output (PLL12_OUT)	This pin can be used as an I/O pin, CLK6n, as the PLL12_OUT pin. Only the EP1S40 and larger devices have this pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
CLK13n, PLL11_OUT	I/O, Input (CLK13n), Output (PLL11_OUT)	This pin can be used as an I/O pin, CLK13n, or used as the PLL11_OUT pin. Only the EP1S40 and larger devices have this pin.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
CRC_ERROR	I/O, Output	Active high indicates that the error detection circuit has detected errors in the configuration RAM cells. This pin is optional and is used when the CRC error detector is enabled. Otherwise, it is a user I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =0) or local update (RUnLU =1) modes. If MSEL2=0, the RUnLU pin is a user I/O pin.



Notes:
1.This is a top view of the silicon die.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

Device	Pin Count	FAST PLL source location	Number of Rx Channels	Number of Tx channels	Number of Overlapped Rx Channels	Number of Overlapped Tx Channels
EP1S80	956	PLL1	20	10	10	10
		PLL2	20	10	10	10
		PLL3	20	10	10	10
		PLL4	20	10	10	10
		PLL7	10	20	10	10
		PLL8	10	20	10	10
		PLL9	10	20	10	10
		PLL10	10	20	10	10
	1508	PLL1	20	20	10	10
		PLL2	20	20	10	10
		PLL3	20	20	10	10
		PLL4	20	20	10	10
		PLL7	24	28	10	10
		PLL8	24	28	10	10
		PLL9	24	28	10	10
		PLL10	24	28	10	10