Pin Name (1)	**144-Pin TQFP**	**208-Pin PQFP** (2)	**240-Pin PQFP** (3)	**324-Pin FineLine BGA**	**356-Pin BGA**
MSEL0 (4)	18	25	29	J17	P1
MSEL1 (4)	19	26	30	J16	P2
nSTATUS (4)	57	82	92	U9	AF15
nCONFIG (4)	22	29	33	K17	R1
DCLK (4)	93	132	152	J3	N25
CONF_DONE (4)	58	83	93	U8	AE15
INIT_DONE (5)	121	178	206	E11	A16
nCE (4)	91	130	150	K2	P26
nCEO (4)	128	185	213	C10	A12
nWS (6)	103	145	164	K5	H22
nRS (6)	102	142	161	J6	H24
nCS (6)	101	141	160	H5	J24
CS (6)	98	138	157	M2	K25
RDYnBSY (6)	120	177	205	E10	B16
CLKUSR (6)	119	176	204	F10	C16
DATA7 (6)	104	146	166	H6	G23
DATA6 (6)	105	150	169	G4	F24
DATA5 (6)	109	157	181	B2	C24
DATA4 (6)	111	160	185	C5	A25
DATA3 (6)	112	163	189	B6	B22
DATA2 (6)	115	168	195	E8	B20
DATA1 (6)	117	173	200	F9	B18
DATA0 (4), (7)	94	133	153	J2	M26
TDI (4)	90	129	149	K3	P25
TDO (4)	123	180	208	C9	B15
TCK (4)	52	76	87	U10	AE12
TMS (4)	51	75	86	U11	AF11
TRST (4)	129	186	214	B10	B12
Dedicated Inputs	56, 53, 124, 127	81, 77, 181, 184	91, 88, 209, 212	B9, D10, T9, T10	A13, A15, AE14, AF12
LOCK (8)	80	119	138	N2	T24
CLK2 (9)	92	131	151	J4	N26
CLK1	20	27	31	K16	P3
DEV_CLRn (5)	97	137	156	L5	L23
DEV_OE (5)	84	124	143	L4	R26
VCCINT	125, 108, 86, 73, 55, 36, 21, 16, 1	182, 156, 126, 105, 79, 52, 28, 23, 1	1, 27, 32, 60, 90, 122, 145, 179, 210	F7, G6, G11, H9, H12, J8, K11, K12, L7, L10, M8, M13, N5, N12	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1, M25, P4, R2, T22, U4, Y26
VCCIO	144, 116, 89, 61, 28	136, 86, 80, 53, 8, 208, 189, 172	12, 45, 67, 97, 120, 148, 177, 199, 229	E6, F5, F12, G8, G13, H7, H10, J11, K8, L9, L12, M6, M11, N7, N14, P6, P13	C26, M22, P22, AD26, AF26, AD14, AD12, AF1, AD1, P5, M5, C1, A1, C12, C14, A26
VCC_CKLK (10)	85	125	144	J7	P23

Pin Name (1)	**144-Pin TQFP**	**208-Pin PQFP** (2)	**240-Pin PQFP** (3)	**324-Pin FineLine BGA**	**356-Pin BGA**
GNDINT	126, 87, 77, 74, 54, 34, 17, 4	183, 143, 127, 118, 78, 39, 24, 16	19, 28, 42, 89, 137, 146, 162, 211	G9, D4, D15, E5, E14, F6, F13, G7, G12, H8, H11, J9, J10, K9, K10, L8, L11, M7, M12, N6, N13, P5, P14, R4, R15	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24
GNDIO (11)	134, 106, 72, 42, 12	199, 169, 149, 114, 95, 64, 43, 10	26, 56, 78, 108, 132, 165, 188, 218, 240	–	–
GND_CKLK (10)	88	128	147	K7	P24
No Connect (N.C.)	–	–	–	–	AA26, AA25, AA3, AA2, AA1, AA24, AA23, AB26, AB2, AB1, AB24, AB23, AB22, AC26, AC25, AC2, AC1, D2, D1, E4, E3, E2, J25, K26, K23
Total User I/O Pins (12)	101	159	189	252	252

Notes:

(1) All pins that are not listed are user I/O pins.
(2) EP20K100 devices in 208-pin PQFP packages are pin-compatible with EP20K200 devices in the same package if pins 154, 148, 121, 109, 48, 36, 11, and 3 are tri-stated and connected to VCCINT, and if pins 153, 147, 110, 47, 35, 12, and 4 are tristated and connected to GNDINT.
(3) EP20K100 devices in 240-pin PQFP packages are pin-compatible with EP20K200 devices in the same package if pins 176, 168, 140, 127, 52, 39, 14, and 5 are tri-stated and connected to VCCINT, and if pins 175, 167, 128, 51, 38, 15, and 6 are tri-stated and connected to GNDINT.
(4) This pin is a dedicated pin; it is not available as a user I/O pin.
(5) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(6) This pin can be used as a user I/O pin after configuration.
(7) This pin is tri-stated in user mode.
(8) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(9) This pin drives the ClockLock and ClockBoost circuitry.
(10) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 2.5-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(11) GNDIO and GNDINT are connected together in BGA packages.
(12) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.