Pin Name (1)	**208-Pin RQFP** (2)	**240-Pin RQFP** (3)	**356-Pin FineLine BGA**	**484-Pin FineLine BGA**
MSEL0 (2)	25	29	P1	L19
MSEL1 (2)	26	30	P2	L18
nSTATUS (2)	82	92	AF15	W11
nCONFIG (2)	29	33	R1	M19
DCLK (2)	132	152	N25	L5
CONF_DONE (2)	83	93	AE15	W10
INIT_DONE (3)	178	206	A16	G13
nCE (2)	130	150	P26	M4
nCEO (2)	185	213	A12	E12
nWS (4)	145	164	H22	M7
nRS (4)	142	161	H24	L8
nCS (4)	141	160	J24	K7
CS (4)	138	157	K25	P4
RDYnBSY (4)	177	205	B16	G12
CLKUSR (4)	176	204	C16	H12
DATA7 (4)	146	166	G23	K8
DATA6 (4)	150	169	F24	J6
DATA5 (4)	157	181	C24	D4
DATA4 (4)	160	185	A25	E7
DATA3 (4)	163	189	B22	D8
DATA2 (4)	168	195	B20	G10
DATA1 (4)	173	200	B18	H11
DATA0 (2), (5)	133	153	M26	L4
TDI (2)	129	149	P25	M5
TDO (2)	180	208	B15	E11
TCK (2)	76	87	AE12	W12
TMS (2)	75	86	AF11	W13
TRST (2)	186	214	B12	D12
Dedicated Inputs	81, 77, 181, 184	91, 88, 209, 212	A13, A15, AF12, AE14	D11, F12, V11, V12
Dedicated Clock Pins	27, 131	31, 151	P3, N26	L6, M18
LOCK (6)	119	138	T24	R4
CLK2 (7)	131	151	N26	L6
DEV_CLRn (3)	137	156	L23	N7
DEV_OE (3)	124	143	R26	N6
VCCINT	1, 3, 11, 23, 28, 36, 48, 52, 79, 105, 109, 121, 126, 148, 154, 156, 182	1, 5, 14, 27, 32, 39, 52, 60, 90, 122, 127, 140, 145, 168, 176, 179, 210	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1,M25, P4, R2, T22, U4, Y26	AA1, AA22, B1, B22, H9, J8, J13, K11, K14, L10, M13, M14, M22, N9, N12, P10, P15, R7, R14
VCCIO	8, 53, 80, 86, 136, 172, 189, 208	12, 45, 67, 97, 120, 148, 177, 199, 229	C26, M22, P22, AD26, AF26, AD14, AD12, AF1, AD1, P5, M5, C1, A1, C12, C14, A26	G8, H7, H14, J10, J15, K9, K12, L1, L13, L22, M10, N11, N14, P8, P13, R9, R16, T8, T15
VCC_CKLK (8)	125	144	P23	L9

Pin Name (1)	**208-Pin RQFP** (2)	**240-Pin RQFP** (3)	**356-Pin FineLine BGA**	**484-Pin FineLine BGA**
GNDINT	4, 12, 16, 24, 35, 39, 47, 78, 110, 118, 127, 143, 147, 153, 183	6, 15, 19, 28, 38, 42, 51, 89, 128, 137, 146, 162, 167, 175, 211	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24	A1, A11, A22, AA2, AA21, AB1, AB11, AB22, B2, B21, F6, F17, G7, G16, H8, H15, J9, J11, J14, K10, K13, L2, L11, L12, M1, M11, M12, M21, N10, N13, P9, P14, R8, R15, T7, T16, U6, U17
GNDIO (9)	10, 43, 64, 95, 114, 149, 169, 199	26, 56, 78, 108, 132, 165, 188, 218, 240	–	–
GND_CKLK (8)	128	147	P24	M9
No Connect (N.C.)	–	–	–	A9, A10, A12, A13, A14, AB9, AB10, AB12, AB13, AB14
Total User I/O Pins (10)	144	174	277	382

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(7) This pin drives the ClockLock and ClockBoost circuitry.
(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 2.5-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(9) GNDIO and GNDINT are connected together in BGA packages.
(10) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.