I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
8	1	I/O	–	–	B11	–	F6	E5
8	2	I/O	155	180	B10	D25	F5	E3
8	3	I/O	–	–	B9	–	F4	F5
8	4	I/O	–	–	A8	E22	C1	F4
–	5	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	6	I/O	–	–	B8	–	D1	E4
8	7	I/O	–	–	A7	–	E2	F3
8	8	I/O	152	178	B7	E24	G6	D5
8	9	I/O	–	–	B6	–	G5	G5
8	10	I/O	–	–	A6	D26	G4	G3
–	11	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	12	I/O	–	174	A5	–	G3	G8
8	13	I/O	–	–	B5	–	F2	G4
8	14	I/O	151	173	B4	F22	E1	C4
8	15	I/O	–	–	A3	–	G2	G6
8	16	I/O	–	–	A4	E25	H6	H5
–	17	GNDINT	GND	GND	GND	GND	GND	GND
8	18	I/O	–	172	C3	–	H4	G7
8	19	I/O	–	–	C1	–	H3	H7
8	20	I/O	–	171	D3	F23	F1	H4
8	21	I/O	–	–	D2	–	H2	H6
8	22	I/O	–	–	C2	E26	G1	K7
–	23	GNDIO	GND	GND	GND	GND	GND	GND
8	24	I/O	–	170	D1	–	J6	J5
8	25	I/O	–	–	B3	–	J5	H9
8	26	I/O, DATA6 (2)	150	169	J6	F24	L6	L8
8	27	I/O	–	–	E3	–	J4	H3
8	28	I/O	–	–	E1	G22	J3	K3
–	29	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	30	I/O	–	–	E6	–	J2	J4
8	31	I/O	–	–	E2	–	J1	K5
8	32	I/O, DATA7 (2)	146	166	K8	G23	M6	M10
8	33	I/O	–	–	A2	–	K6	L6
8	34	I/O	–	–	E4	F25	K5	J7
–	35	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	36	I/O	–	–	F3	F26	K4	J3
8	37	I/O	–	–	E5	–	K3	K8
8	38	I/O, nWS (2)	145	164	M7	H22	M1	P9
8	39	I/O	–	–	F5	–	K2	K6
8	40	I/O	–	–	F2	G24	K1	K4
–	41	GNDINT	GND	GND	GND	GND	GND	GND
8	42	I/O	–	–	F4	H23	L5	N5
8	43	I/O	–	–	H5	–	L4	M8
8	44	I/O	144	163	G3	G25	L2	J8
8	45	I/O	–	–	F7	–	L1	M6
8	46	I/O	–	–	G6	G26	M5	L7
–	47	GNDIO	GND	GND	GND	GND	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
8	48	I/O	–	–	F1	J22	M4	L9
8	49	I/O	–	–	H1	–	M3	M7
8	50	I/O, nRS (2)	142	161	L8	H24	N1	N10
8	51	I/O	–	–	G2	–	M2	L5
8	52	I/O	–	–	H3	H25	N6	P8
–	53	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	54	I/O	–	–	G4	H26	N5	L4
8	55	I/O	–	–	J4	–	N3	L3
8	56	I/O, nCS (2)	141	160	K7	J24	P2	M9
8	57	I/O	–	–	G5	–	N2	R4
8	58	I/O	–	–	G1	K22	P6	M5
–	59	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	60	I/O	–	–	H6	J25	P5	M3
8	61	I/O	–	–	H4	–	P4	P4
8	62	I/O	–	–	H2	K23	P3	J6
8	63	I/O	–	–	L3	–	P1	R3
8	64	I/O	–	–	K6	J26	R6	P5
–	65	GNDINT	GND	GND	GND	GND	GND	GND
–	66	VCC_CKLK4 (3)	140	159	M8	K24	R4	P10
–	67	GND_CKLK4 (3)	139	158	N8	L22	R3	R10
–	68	GND_CKLK4 (3)	139	158	N8	L22	R3	R10
8	69	I/O, CS (2)	138	157	P4	K25	R2	T6
8	70	I/O	–	–	K4	K26	R1	M4
8	71	I/O, DEV_CLRn (4)	137	156	N7	L23	T6	R9
–	72	VCCIO	VCCIO8	VCCIO8	–	VCCIO8	VCCIO8	–
–	73	GNDIO	GND	GND	GND	GND	GND	GND
8	74	I/O, CLKLK_FB2n (5)	–	–	P6	L24	T5	T8
–	75	CLKLK_FB2p	135	155	R6	L25	T4	U8
8	76	I/O, CLK4n (5)	–	–	N5	L26	T3	R7
–	77	CLK4p	134	154	N4	M23	T2	R6
8	78	I/O, CLK2n (5)	–	–	L7	M24	T1	N9
–	79	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	80	DATA0 (6), (7)	133	153	L4	M26	U4	N6
–	81	DCLK (6)	132	152	L5	N25	U3	N7
–	82	CLK2p	131	151	L6	N26	U2	N8
–	83	NCE (6)	130	150	M4	P26	U1	P6
–	84	TDI (6)	129	149	M5	P25	W1	P7
–	85	VCCIO	VCCIO7	VCCIO7	–	VCCIO7	VCCIO7	–
–	86	GND_CKLK2 (3)	128	147	M9	P24	W2	P11
–	87	GND_CKLK2 (3)	128	147	M9	P24	W2	P11
–	88	GNDINT	GND	GND	GND	GND	GND	GND
–	89	VCC_CKLK2 (3)	125	144	L9	P23	W4	N11
7	90	I/O, DEV_OE (4)	124	143	N6	R26	Y5	R8
–	91	VCC_CKOUT2 (8)	123	142	T5	R25	Y1	V7

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
–	92	GND_CKOUT2 (8)	122	141	T4	R24	Y2	V6
–	93	CLKLK_OUT2p (9)	120	139	P5	R23	Y3	T7
7	94	I/O, CLKLK_OUT2n (5)	–	–	R5	R22	Y4	U7
–	95	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	96	I/O	–	–	J5	T26	W5	D1
7	97	I/O	–	–	J7	T25	Y6	D2
7	98	I/O, LOCK2 (10)	119	138	R4	T24	AB6	U6
7	99	I/O	–	–	K5	T23	AA2	E1
7	100	I/O	–	–	J3	U26	AA3	E2
–	101	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	102	I/O	–	–	M6	U25	AA5	F1
7	103	I/O	–	–	J2	–	AA6	F2
7	104	I/O	–	–	J1	U24	AB1	R5
7	105	I/O	–	–	N2	–	AB2	G1
7	106	I/O	–	–	K3	V26	AB3	G2
–	107	GNDIO	GND	GND	GND	GND	GND	GND
7	108	I/O	117	136	K1	U23	AB4	H1
7	109	I/O	–	–	M2	–	AB5	H2
7	110	I/O, LOCK4 (10)	116	135	U5	V25	AC6	W7
7	111	I/O	–	–	N1	–	AC1	J1
7	112	I/O	–	–	M3	U22	AC2	J2
–	113	GNDINT	GND	GND	GND	GND	GND	GND
7	114	I/O	–	–	K2	V24	AC4	K1
7	115	I/O	–	–	N3	–	AC5	K2
7	116	I/O	–	134	P3	W26	AA1	T5
7	117	I/O	–	–	P1	–	AD1	L1
7	118	I/O	–	–	R3	V23	AD2	L2
–	119	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	120	I/O	–	–	P2	W25	AD3	M1
7	121	I/O	–	–	R2	–	AD4	M2
7	122	I/O	–	–	R1	V22	AD5	T3
7	123	I/O	–	133	T1	–	AD6	R1
7	124	I/O	–	–	U3	W24	AE1	R2
–	125	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	126	I/O	–	–	U4	W23	AE3	T1
7	127	I/O	–	–	T3	–	AE4	T2
7	128	I/O	–	131	T2	Y25	AE5	U5
7	129	I/O	–	–	U2	–	AE6	U1
7	130	I/O	–	130	U1	Y24	AF1	U2
–	131	GNDIO	GND	GND	GND	GND	GND	GND
7	132	I/O	–	–	V3	W22	AF2	V1
7	133	I/O	–	–	Y3	–	AF3	V2
7	134	I/O	113	129	W3	AA26	AF4	T4
7	135	I/O	–	–	V4	–	AF5	W1

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
7	136	I/O	–	–	W4	AA25	AF6	W2
–	137	GNDINT	GND	GND	GND	GND	GND	GND
7	138	I/O	–	–	W5	Y23	AH1	Y1
7	139	I/O	–	–	Y4	–	AG2	Y2
7	140	I/O	112	126	Y2	AA24	AG3	U4
7	141	I/O	–	–	W2	–	AG4	AA1
7	142	I/O	–	–	AA3	Y22	AG5	AA2
–	143	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	144	I/O	–	–	V2	AA23	AG6	AB1
7	145	I/O	–	–	Y1	–	AJ1	AB2
7	146	I/O	111	125	V1	AB26	AH2	W4
7	147	I/O	–	–	AB2	–	AK1	AC1
7	148	I/O	–	–	W1	–	AH3	AC2
–	149	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	150	I/O	–	–	AB3	AA22	AH5	U3
7	151	I/O	–	–	AB4	–	AH6	V3
7	152	I/O	108	124	AA4	AB24	AJ2	W5
7	153	I/O	–	–	AA5	–	AL1	W6
7	154	I/O	–	–	AB5	–	AK2	V5
–	155	GNDIO	GND	GND	GND	GND	GND	GND
7	156	I/O	–	–	AA6	AC26	AJ3	V4
7	157	I/O	–	–	AB6	–	AJ4	W3
7	158	I/O	107	123	AA7	AB23	AJ5	Y5
7	159	I/O	–	–	AB7	–	AJ6	AB5
7	160	I/O	–	–	AA8	–	AM1	AA5
–	161	GNDINT	GND	GND	GND	GND	GND	GND
7	162	I/O	–	–	AA11	AC25	AK3	Y6
7	163	I/O	–	–	AA10	–	AK4	AA6
7	164	I/O	106	121	AB8	AB22	AK5	AA7
7	165	I/O	–	–	AA9	–	AK6	AB6
–	166	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	–
–	167	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	168	I/O	104	119	Y5	AD24	AR8	AB7
6	169	I/O	–	118	V5	AE25	AN11	Y7
6	170	I/O	103	117	Y6	AD23	AP10	AB8
6	171	I/O	102	116	T6	AD22	AR9	V8
6	172	I/O	–	–	P7	AF25	AL13	T9
6	173	I/O	101	115	W7	AE24	AM13	AA9
6	174	I/O	–	–	W6	AE23	AN12	AA8
6	175	I/O	100	114	V6	AD21	AP11	Y8
6	176	I/O	99	113	V7	AF24	AL14	Y9
6	177	I/O	–	112	U7	AE22	AR10	W9
–	178	GNDIO	GND	GND	GND	GND	GND	GND
6	179	I/O	98	111	Y7	AF23	AN13	AB9
6	180	I/O	97	110	U8	AD20	AP12	W10
6	181	I/O	96	109	V8	AF22	AM14	Y10
6	182	I/O	–	–	W8	AE21	AR11	AA10

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
6	183	I/O	94	107	Y9	AF21	AL15	AB11
6	184	I/O	–	106	T9	AD19	AN14	V11
6	185	I/O	93	105	Y8	AE20	AP13	AB10
6	186	I/O	–	104	W9	AF20	AR12	AA11
6	187	I/O	92	103	V9	AD18	AR13	Y11
6	188	I/O	–	–	U9	AE19	AM15	W11
–	189	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	190	I/O	91	102	T10	AF19	AN15	V12
6	191	I/O	90	101	U10	AE18	AL16	W12
6	192	I/O	–	–	V10	AD17	AP14	Y12
6	193	I/O	89	100	P11	AF18	AR14	T13
6	194	I/O	88	99	U12	AE17	AP15	W14
6	195	I/O	87	98	Y10	AD16	AR15	AB12
–	196	VCCIO	VCCIO6	VCCIO6	–	VCCIO6	VCCIO6	VCCIO6
6	197	I/O	85	96	R11	AF17	AM16	U13
6	198	I/O	84	95	R10	AE16	AN16	U12
6	199	I/O	–	–	U11	AF16	AP16	W13
6	200	I/O	–	94	T11	AD15	AR16	V13
–	201	CONF_DONE (6)	83	93	W10	AE15	AM17	AA12
–	202	NSTATUS (6)	82	92	W11	AF15	AN17	AA13
5	203	FAST4	81	91	V11	AE14	AP17	Y13
–	204	VCCIO	VCCIO5	VCCIO5	–	VCCIO5	VCCIO5	VCCIO5
–	205	GNDINT	GND	GND	GND	GND	GND	GND
–	206	GNDINT	GND	GND	GND	GND	GND	GND
–	207	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	208	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	209	GNDINT	GND	GND	GND	GND	GND	GND
–	210	GNDINT	GND	GND	GND	GND	GND	GND
–	211	GNDIO	GND	GND	GND	GND	GND	GND
5	212	FAST3	77	88	V12	AF12	AP19	Y14
–	213	TCK (6)	76	87	W12	AE12	AN19	AA14
–	214	TMS (6)	75	86	W13	AF11	AM19	AA15
5	215	I/O	74	85	Y11	AE11	AR20	AB13
5	216	I/O	73	84	T12	AF10	AP20	V14
5	217	I/O	–	83	Y12	AD11	AN20	AB14
5	218	I/O	72	82	V13	AE10	AM20	Y15
5	219	I/O	–	–	R12	AF9	AR21	U14
5	220	I/O	71	81	T13	AD10	AP21	V15
5	221	I/O	–	80	Y13	AE9	AR22	AB15
5	222	I/O	70	79	U13	AF8	AP22	W15
5	223	I/O	69	77	Y14	AD9	AL20	AB16
5	224	I/O	68	76	P12	AE8	AN21	T14
–	225	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
5	226	I/O	67	75	W14	AF7	AM21	AA16
5	227	I/O	66	74	V14	AE7	AR23	Y16
5	228	I/O	–	–	U14	AD8	AR24	W16
5	229	I/O	65	73	R13	AF6	AP23	U15

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
5	230	I/O	–	–	Y15	AE6	AN22	AB17
5	231	I/O	63	72	T14	AD7	AL21	V16
5	232	I/O	62	71	W15	AF5	AR25	AA17
5	233	I/O	–	70	Y16	AE5	AM22	AB18
5	234	I/O	61	69	V15	AD6	AP24	Y17
5	235	I/O	60	68	W16	AF4	AN23	AA18
–	236	GNDIO	GND	GND	GND	GND	GND	GND
–	237	VCCIO	VCCIO5	VCCIO5	–	VCCIO5	VCCIO5	VCCIO5
5	238	I/O	59	66	U15	AE4	AR26	W17
5	239	I/O	–	–	V16	AF3	AL22	Y18
5	240	I/O	58	65	U16	AD5	AP25	W18
5	241	I/O	–	–	W17	AE3	AN24	AA19
5	242	I/O	57	64	V17	AF2	AM23	Y19
5	243	I/O	–	–	U18	AD4	AL23	W20
5	244	I/O	56	63	V18	AE2	AR27	Y20
5	245	I/O	55	62	Y18	AD3	AP26	AB20
5	246	I/O	–	–	Y17	AC5	AN25	AB19
5	247	I/O	54	61	W18	AC4	AR28	AA20
–	248	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
–	249	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	250	I/O	–	–	AA12	–	AL33	AA21
4	251	I/O	51	59	AB15	AA5	AK30	Y22
4	252	I/O	–	–	AB16	–	AK31	AB21
4	253	I/O	–	–	AA13	AC2	AK32	U19
–	254	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	255	I/O	–	–	AB17	–	AL34	AB22
4	256	I/O	–	–	AA14	–	AM35	V19
4	257	I/O	50	58	AA15	AC1	AJ30	T18
4	258	I/O	–	–	AB18	–	AJ31	W21
4	259	I/O	–	57	AA16	AA4	AJ32	V20
–	260	GNDIO	GND	GND	GND	GND	GND	GND
4	261	I/O	–	–	AB19	–	AJ33	V21
4	262	I/O	–	–	AB20	–	AK34	Y21
4	263	I/O	49	–	AA17	AB2	AL35	W22
4	264	I/O	–	55	AA18	–	AJ34	AA22
4	265	I/O	–	–	AB21	Y5	AH30	U20
–	266	GNDINT	GND	GND	GND	GND	GND	GND
4	267	I/O	–	–	Y22	AB1	AH32	R17
4	268	I/O	–	–	AA20	–	AH33	W23
4	269	I/O	46	54	AA19	AA3	AK35	T19
4	270	I/O	–	–	V21	–	AH34	U21
4	271	I/O	–	–	V22	Y4	AJ35	P17
–	272	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	273	I/O	–	–	W21	AA2	AG30	R18
4	274	I/O	–	–	W22	–	AG31	W24
4	275	I/O	45	53	Y21	AA1	AG32	T20
4	276	I/O	–	–	W19	–	AG33	V24

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
4	277	I/O	–	–	V20	W5	AG34	N16
–	278	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	279	I/O	–	50	Y19	Y3	AG35	V22
4	280	I/O	–	–	R17	–	AF30	R19
4	281	I/O	44	49	Y20	W4	AF31	V23
4	282	I/O	–	–	T17	–	AF32	P18
4	283	I/O	–	–	P16	Y2	AF33	N17
–	284	GNDIO	GND	GND	GND	GND	GND	GND
4	285	I/O	–	–	U19	Y1	AF34	T21
4	286	I/O	–	–	T18	–	AF35	R21
4	287	I/O	–	48	T19	V5	AE30	U22
4	288	I/O	–	–	V19	–	AE31	R20
4	289	I/O	–	–	U20	W3	AE32	P22
–	290	GNDINT	GND	GND	GND	GND	GND	GND
4	291	I/O	–	–	W20	V4	AE34	N18
4	292	I/O	–	–	R18	–	AE35	U23
4	293	I/O	–	47	N15	W2	AD30	N19
4	294	I/O	–	–	U21	–	AD31	N22
4	295	I/O	–	46	P17	W1	AD32	L20
–	296	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	297	I/O	–	–	R19	V3	AD33	M17
4	298	I/O	–	–	M15	–	AD34	T22
4	299	I/O	41	44	N16	U5	AD35	M18
4	300	I/O	–	–	U22	–	AC30	T23
4	301	I/O	40	43	P18	V2	AC31	R23
–	302	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	303	I/O	–	–	T22	V1	AC33	U24
4	304	I/O	–	–	L14	–	AC34	R24
4	305	I/O	38	41	T20	U3	AC35	T24
4	306	I/O	–	–	N17	–	AB30	M21
4	307	I/O	–	–	T21	T5	AB31	M24
–	308	GNDIO	GND	GND	GND	GND	GND	GND
4	309	I/O	–	–	M16	U2	AB32	M22
4	310	I/O	–	–	L15	–	AB33	R22
4	311	I/O	37	40	P19	T4	AB34	M23
4	312	I/O	–	–	N19	–	AB35	L22
4	313	I/O	–	–	R20	U1	AA30	L21
–	314	GNDINT	GND	GND	GND	GND	GND	GND
4	315	I/O	–	–	N18	–	AA32	L23
4	316	I/O	–	–	M20	T3	AA33	L24
4	317	I/O	–	–	L16	–	AA34	N23
4	318	I/O	34	37	R21	T2	AA35	AF18
4	319	I/O	33	36	L17	R5	Y30	AE18
–	320	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	–
4	321	I/O	–	–	L20	–	Y31	AF20
4	322	I/O	32	35	J18	–	Y32	AE20
4	323	I/O, CLK3n (5)	–	–	K18	T1	Y33	M20

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
–	324	CLK3p	31	34	K17	R4	Y34	M19
4	325	I/O, CLK1n (5)	30	–	M17	R3	Y35	P19
–	326	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	327	nCONFIG (6)	29	33	M19	R1	W32	P21
–	328	CLKLK_ENA (6), (11)	28	32	M14	P4	W33	P16
–	329	CLK1p	27	31	M18	P3	W34	P20
–	330	MSEL1 (6)	26	30	L18	P2	W35	N20
–	331	MSEL0 (6)	25	29	L19	P1	U35	N21
–	332	GNDINT	GND	GND	GND	GND	GND	GND
3	333	I/O	22	25	K15	N2	U33	AF22
3	334	I/O	–	–	P20	–	U32	AE22
3	335	I/O	–	–	K16	N1	U31	AE23
3	336	I/O	–	–	P21	–	T35	AF23
3	337	I/O	–	–	N21	M1	T34	AC26
–	338	GNDIO	GND	GND	GND	GND	GND	GND
3	339	I/O	–	–	R22	M2	T33	AC25
3	340	I/O	–	–	N22	–	T32	AB25
3	341	I/O	21	24	P22	M3	T31	AB26
3	342	I/O	–	–	K19	–	T30	J23
3	343	I/O	–	–	K22	M4	R35	L19
–	344	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	345	I/O	20	23	K20	L2	R33	AA25
3	346	I/O	–	–	N20	–	R32	AA26
3	347	I/O	19	22	K21	L3	R31	L18
3	348	I/O	–	–	J20	–	R30	Y25
3	349	I/O	–	–	J19	L4	P35	Y26
–	350	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	351	I/O	18	21	J21	L5	P34	W25
3	352	I/O	–	–	J22	–	P33	W26
3	353	I/O	17	20	L21	K1	P32	J24
3	354	I/O	–	–	G21	–	P31	V25
3	355	I/O	–	–	J17	K2	P30	V26
–	356	GNDINT	GND	GND	GND	GND	GND	GND
3	357	I/O	15	18	J16	K3	N34	U25
3	358	I/O	–	–	G22	–	N33	U26
3	359	I/O	14	17	H19	J1	N32	K21
3	360	I/O	–	–	H21	–	N31	T25
3	361	I/O	–	–	H18	K4	N30	T26
–	362	GNDIO	GND	GND	GND	GND	GND	GND
3	363	I/O	–	–	H20	J2	M35	R25
3	364	I/O	–	–	H22	–	M34	R26
3	365	I/O	13	16	F22	K5	M33	K23
3	366	I/O	–	–	H17	–	M32	M25
3	367	I/O	–	–	G18	J3	M31	M26
–	368	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	369	I/O	–	–	E20	J4	L35	L25

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
3	370	I/O	–	–	F18	–	L34	L26
3	371	I/O	9	13	F20	H2	L33	K20
3	372	I/O	–	–	G20	–	L32	K25
3	373	I/O	–	–	E22	J5	L31	K26
–	374	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	375	I/O	–	–	F19	H3	L30	J25
3	376	I/O	–	–	E19	–	K35	J26
3	377	I/O	7	11	G19	G1	K34	K22
3	378	I/O	–	–	D20	–	K33	H25
3	379	I/O	–	–	E18	H4	K32	H26
–	380	GNDINT	GND	GND	GND	GND	GND	GND
3	381	I/O	–	–	D19	G2	K30	G25
3	382	I/O	–	–	C20	–	J35	G26
3	383	I/O	–	10	C21	G3	H35	K24
3	384	I/O	–	–	B20	–	J34	F25
3	385	I/O	–	9	D22	H5	J33	F26
–	386	GNDIO	GND	GND	GND	GND	GND	GND
3	387	I/O	–	–	C22	F1	J32	E25
3	388	I/O	–	–	F21	–	J31	E26
3	389	I/O	–	8	A21	G4	J30	H24
3	390	I/O	–	–	E21	–	G35	D25
3	391	I/O	–	7	D21	F2	H34	D26
–	392	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	393	I/O	–	–	A20	F3	H33	K19
3	394	I/O	–	–	B19	–	H32	J20
3	395	I/O	6	4	A19	G5	H31	G22
3	396	I/O	–	–	B18	–	H30	H20
3	397	I/O	–	–	A18	F4	G34	H22
–	398	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	399	I/O	–	–	B17	E2	E35	J22
3	400	I/O	–	–	A17	–	F34	G24
3	401	I/O	5	3	B16	D1	G33	H21
3	402	I/O	–	–	A16	–	G32	G21
3	403	I/O	–	–	B15	E3	G31	J21
–	404	GNDINT	GND	GND	GND	GND	GND	GND
3	405	I/O	–	–	A15	F5	D35	F22
3	406	I/O	–	–	B14	D2	E34	G20
3	407	I/O	2	2	B13	E4	F33	F21
3	408	I/O	–	–	B12	–	F32	E22
–	409	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2	VCCIO2
–	410	GNDIO	GND	GND	GND	GND	GND	GND
2	411	I/O	207	239	C19	B2	A28	E21
2	412	I/O	–	238	D18	C3	C25	F20
2	413	I/O	206	237	C18	D5	B26	E20
2	414	I/O	–	–	G17	A2	A27	J19
2	415	I/O	205	236	E17	C4	E23	G19
2	416	I/O	–	–	D17	B3	D23	F19

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
2	417	I/O	204	235	C17	A3	C24	E19
2	418	I/O	–	–	H16	C5	B25	K18
2	419	I/O	203	234	F16	B4	E22	H18
2	420	I/O	202	233	E16	A4	A26	G18
–	421	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2
2	422	I/O	201	232	C16	C6	C23	E18
2	423	I/O	200	231	D16	B5	B24	F18
2	424	I/O	198	230	C15	C7	D22	E17
2	425	I/O	–	–	D15	B6	A25	F17
–	426	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2	VCCIO2
2	427	I/O	197	228	E15	A5	E21	G17
2	428	I/O	–	–	F15	C8	C22	H17
2	429	I/O	196	227	D14	B7	B23	F16
2	430	I/O	195	226	G15	A6	A24	J17
2	431	I/O	–	225	C14	A7	A23	E16
2	432	I/O	194	224	E14	B8	D21	G16
–	433	GNDIO	GND	GND	GND	GND	GND	GND
2	434	I/O	193	223	F14	C9	C21	H16
2	435	I/O	192	222	C13	A8	E20	E15
2	436	I/O	–	221	D13	B9	B22	F15
2	437	I/O	191	220	C12	C10	A22	E14
2	438	I/O	–	–	F13	A9	B21	H15
2	439	I/O	190	219	C11	B10	A21	E13
–	440	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2	–
2	441	I/O	–	–	J12	C11	D20	L14
2	442	I/O	188	217	E13	A10	C20	G15
2	443	I/O	–	216	H13	B11	B20	K15
2	444	I/O	187	215	G14	A11	A20	J16
–	445	TRST (6)	186	214	D12	B12	D19	F14
–	446	NCEO (6)	185	213	E12	A12	C19	G14
1	447	FAST1	184	212	F12	A13	B19	H14
–	448	GNDINT	GND	GND	GND	GND	GND	GND
–	449	GNDINT	–	–	–	–	–	–
–	450	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	451	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	452	GNDINT	GND	GND	GND	GND	GND	GND
–	453	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	454	FAST2	181	209	D11	A15	B17	F13
–	455	TDO (6)	180	208	E11	B15	C17	G13
–	456	GNDINT	–	–	GND	–	GND	GND
1	457	I/O	179	207	F11	C15	A16	H13
1	458	I/O, INITDONE (4)	178	206	G13	A16	C16	J15
1	459	I/O, RDYNBSY (2)	177	205	G12	B16	A14	J14
1	460	I/O	–	–	D10	A17	B16	F12
1	461	I/O, CLKUSR (2)	176	204	H12	C16	C15	K14
1	462	I/O	–	203	C10	B17	D16	E12

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
1	463	I/O	175	202	C9	A18	A15	E11
1	464	I/O	174	201	G11	C17	B15	J13
1	465	I/O, DATA1 (2)	173	200	H11	B18	C13	K13
1	466	I/O	–	–	F10	A19	E16	H12
–	467	GNDIO	GND	GND	GND	GND	GND	GND
–	468	VCCIO	VCCIO1	VCCIO1	–	VCCIO1	VCCIO1	VCCIO1
1	469	I/O	171	198	C8	B19	B14	E10
1	470	I/O	–	197	D9	C18	D15	F11
1	471	I/O	170	196	E10	A20	A13	G12
1	472	I/O, DATA2 (2)	168	195	G10	B20	A8	J12
1	473	I/O	167	–	E9	C19	A12	G11
1	474	I/O	166	194	C7	A21	B13	E9
1	475	I/O	165	193	D7	A22	C14	F9
1	476	I/O	164	192	H10	B21	E15	K12
1	477	I/O	–	–	F9	C20	A11	H11
1	478	I/O	–	191	C6	A23	D14	E8
–	479	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	480	I/O	–	190	D6	A24	B12	F8
1	481	I/O, DATA3 (2)	163	189	D8	B22	B7	F10
1	482	I/O	162	187	C5	B23	A10	E7
1	483	I/O	161	186	E8	C21	E14	G10
1	484	I/O	–	–	F8	B24	B11	H10
1	485	I/O, DATA4 (2)	160	185	E7	A25	B5	G9
1	486	I/O	159	184	G9	C22	C12	J11
1	487	I/O	158	183	D5	C23	D13	F7
1	488	I/O	–	182	C4	B25	E13	E6
1	489	I/O, DATA5 (2)	157	181	D4	C24	E7	F6
–	490	GNDIO	GND	GND	GND	GND	GND	GND

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
MSEL0 (6)	25	29	P1	L19	U35	N21
MSEL1 (6)	26	30	P2	L18	W35	N20
nSTATUS (6)	82	92	AF15	W11	AN17	AA13
nCONFIG (6)	29	33	R1	M19	W32	P21
DCLK (6)	132	152	N25	L5	U3	N7
CONF_DONE (6)	83	93	AE15	W10	AM17	AA12
INIT_DONE (4)	178	206	A16	G13	C16	J15
nCE (6)	130	150	P26	M4	U1	P6
nCEO (6)	185	213	A12	E12	C19	G14
nWS (2)	145	164	H22	M7	M1	P9
nRS (2)	142	161	H24	L8	N1	N10
nCS (2)	141	160	J24	K7	P2	M9
CS (2)	138	157	K25	P4	R2	T6
RDYnBSY (2)	177	205	B16	G12	A14	J14
CLKUSR (2)	176	204	C16	H12	C15	K14
DATA7 (2)	146	166	G23	K8	M6	M10
DATA6 (2)	150	169	F24	J6	L6	L8
DATA5 (2)	157	181	C24	D4	E7	F6
DATA4 (2)	160	185	A25	E7	B5	G9
DATA3 (2)	163	189	B22	D8	B7	F10
DATA2 (2)	168	195	B20	G10	A8	J12
DATA1 (2)	173	200	B18	H11	C13	K13
DATA0 (6), (7)	133	153	M26	L4	U4	N6
TDI(6)	129	149	P25	M5	W1	P7
TDO (6)	180	208	B15	E11	C17	G13
TCK (6)	76	87	AE12	W12	AN19	AA14
TMS (6)	75	86	AF11	W13	AM19	AA15
TRST (6)	186	214	B12	D12	D19	F14
Dedicated Fast I/O Pins	77, 81, 181, 184	88, 91, 209, 212	A13, A15, AF12, AE14	D11, F12, V11, V12	B17, B19, AP17, AP19	F13, H14, Y13, Y14
CLK1p	27	31	P3	M18	W34	P20
CLK2p	131	151	N26	L6	U2	N8
CLK3p	31	34	R4	K17	Y34	M19
CLK4p	134	154	M23	N4	T2	R6
LOCK2 (10)	119	138	T24	R4	AB6	U6
LOCK4 (10)	116	135	V25	U5	AC6	W7
CLKLK_ENA (6), (11)	28	32	P4	M14	W33	P16
CLKLK_OUT2p (9)	120	139	R23	P5	Y3	T7
CLKLK_FB2p	135	155	L25	R6	T4	U8
DEV_CLRn (4)	137	156	L23	N7	T6	R9
DEV_OE (4)	124	143	R26	N6	Y5	R8

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
VCCINT	36, 23, 11, 3, 1, 182, 156, 154, 148, 126, 121, 109, 105, 79, 52, 48	39, 27, 14, 5, 1, 210, 179, 176, 168, 145, 140, 127, 122, 90, 60, 52	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1, M25, R2, T22, U4, Y26	B1, B22, H9, J8, J13, K11, K14 L10, M13, M22, N9, N12, P10, P15, R7, R14, AA1, AA22	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO1	172	199	C14, A26,	G8, J10	C4, D5, E17	A6, J10, L12
VCCIO2	208,189	229	A1, C12,	H14, K12	E19, D31, C32	A13, K16, M14
VCCIO3	8	12	M5, C1	J15, L13	F30, F31, U30	A21, L17, N15
VCCIO4	42	45	AD1, P5	L22, N14, R16	W30, AL31, AL32	N24, R16, U18
VCCIO5	80, 53	67	AD12, AF1	P13, T15	AN32, AN33, AL19	T15, V17, AF21
VCCIO6	86	120, 97	AF26, AD14	N11, R9, T8	AL17, AM5, AN4	R13, U11, V10, AF13
VCCIO7	115	148	P22, AD26	M10, P8	AL3, AL4, W6	P12, T10, AF6
VCCIO8	136	177	C26, M22	H7, K9, L1	U6, E3, E4	K9, M11, N3
VCC_CKLK2 (3)	125	144	P23	L9	W4	N11
VCC_CKLK4 (3)	140	159	K24	M8	R4	P10
VCC_CKOUT2 (8)	123	142	R25	T5	Y1	V7

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
GND	43, 39, 35, 24, 16, 12, 10, 4, 199, 183, 169, 153, 149, 147, 143, 127, 118, 114, 110, 95, 78, 64, 47	175, 167, 165, 162, 146, 137, 132, 128, 108, 89, 78, 56, 51, 42, 38, 28, 26, 19, 15, 6, 240, 218, 211, 188	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24	A1, A11, A22, B2, B21, F6, F17, G7, G16, H8, H15, J9, J11, J14, K10, K13, L2, L11, L12, M1, M11, M12, M21, N10, N13, P9, P14, R8, R15, T7, T16, U6, U17, AA2, AA21,AB1, AB11, AB22	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D17, D18, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6, V35	A2, A8, A14, A19, A25, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N25, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19
GND_CKLK2 (3)	128	147	P24	M9	W2	P11
GND_CKLK4 (3)	139	158	L22	N8	R3	R10
GND_CKOUT2 (8)	122	141	R24	T4	Y2	V6

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
No Connect (N.C.)				A9, A10, A12, A13, A14, AB9, AB10, AB12, AB13, AB14	A2, A29, A3, A30, A31, A32, A33, A34, A4, A5, A6, A7, A9, AL10, AL11, AL25, AL26, AL27, AL28, AL29, AL7, AL8, AL9, AM10, AM11, AM25, AM26, AM27, AM28, AM29, AM30, AM6 AM7, AM8, AM9, AN10, AN26, AN27, AN28, AN29, AN30, AN31, AN5, AN6, AN7, AN8, AN9, AP27, AP28, AP29, AP3, AP30, AP31, AP32, AP33, AP4, AP5, AP6, AP7, AP8, AP9, AR2, AR29, AR3, AR30, AR31, AR32, AR33 AR34, AR4, AR5, AR6, AR7, B10, B27, B28, B29, B3, B30, B31, B32, B33, B4, B6, B8, B9, C10, C11, C26, C27, C28, C29, C30, C31, C5, C6, C7, C8, C9, D10, D11, D25, D26, D27, D28, D29, D30, D6, D7, D8, D9, E10, E11, E25, E26, E27, E28, E29, E8, E9	A4, A5, A7, A9, A10, A11, A12, A15, A16, A17, A18, A20,A22, A23, B4, B5, B7, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B20, B22, B23, C5, C6, C7, C8, C9, C10, C11, C12, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, E23, E24, F23, F24, G23, H23, Y3, Y4, Y23, Y24, AA3, AA4, AA23, AA24, AB3, AB4, AB23, AB24, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AE4, AE5, AE7, AE9, AE10, AE11, AE12, AE13, AE14, AE15, AE16, AE17, AF4, AF5, AF7, AF9, AF10, AF11, AF12, AF15, AF16, AF17
Total User I/O Pins (12)	136	168	271	376	376	376

Notes:

(1) For the 144-pin, 208-pin, and 240-pin PQFP packages, four unique VCCIO levels are supported. The VCCIO pins for I/O banks 1 and 8 must be at the same level. The VCCIO pins for banks 6 and 7 must be at the same level. The VCCIO pins for I/O banks 4 and 5 must be at the same level. The VCCIO pins for I/O banks 2 and 3 must be at the same level. However, unique VREF settings are supported for each of the eight I/O banks.

(2) This pin can be used as a user I/O pin after configuration.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(6) This pin is a dedicated pin; it is not available as a user I/O pin.

(7) This pin is tri-stated in user mode.

(8) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(9) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(10) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(11) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(12) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.