I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA
8	1	I/O, DATA6 (2)	105	150	B2	G4
-	2	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	3	I/O, DATA7 (2)	104	146	C1	H6
8	4	I/O, nWS (2)	103	145	C2	K5
8	5	I/O, nRS (2)	102	142	D2	J6
-	6	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	7	I/O, nCS (2)	101	141	D3	H5
-	8	VCC_CKLK4 (3)	100	140	D4	K6
-	9	GND_CKLK4 (3)	99	139	E2	L6
-	10	GND_CKLK4 (3)	99	139	E2	L6
8	11	I/O, CS (2)	98	138	E3	M2
8	12	I/O, DEV_CLRn (4)	97	137	E4	L5
-	13	GNDINT	GND	GND	GND	GND
8	14	I/O, CLKLK_FB2n (5)	-	-	F5	M4
-	15	CLKLK_FB2p	96	135	F4	N4
8	16	I/O, CLK4n (5)	-	-	F3	L3
8	17	CLK4p	95	134	F2	L2
8	18	I/O, CLK2n (5)	-	-	G4	J5
-	19	DATA0 (6), (7)	94	133	G3	J2
-	20	DCLK (6)	93	132	G2	J3
8	21	CLK2p	92	131	G7	J4
-	22	nCE (6)	91	130	H5	K2
-	23	TDI (6)	90	129	H2	K3
-	24	GNDIO	GND	GND	GND	GND
-	25	GND_CKLK2 (3)	88	128	G5	K7
-	26	GND_CKLK2 (3)	88	128	G5	K7
-	27	VCC_CKLK2 (3)	85	125	G6	J7
7	28	I/O, DEV_OE (4)	84	124	J3	L4
-	29	VCC_CKOUT2 (8)	83	123	H4	P3
-	30	GND_CKOUT2 (8)	82	122	H3	P2
7	31	I/O, CLKLK_OUT2n (5)	-	121	K2	N3
-	32	CLKLK_OUT2p	81	120	J2	M3
-	33	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	34	I/O, LOCK2 (9)	80	119	K3	N2
7	35	I/O	79	117	J4	H4
7	36	I/O, LOCK4 (9)	78	116	L2	R3
7	37	I/O	76	113	L1	H2
7	38	I/O	75	112	L3	G5
-	39	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	40	I/O	-	111	-	H3
7	41	I/O	-	110	-	G1
7	42	I/O	-	109	-	H1
7	43	I/O	-	108	-	K1
-	44	GNDINT	GND	GND	GND	GND
-	45	GNDIO	GND	GND	GND	GND
-	46	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	47	I/O	71	104	L4	U5
6	48	I/O	-	103	-	U4
6	49	I/O	70	102	K4	T4
6	50	I/O	69	101	J5	R5
-	51	GNDIO	GND	GND	GND	GND
6	52	I/O	68	100	K5	V5
6	53	I/O	-	99	-	R6
6	54	I/O	67	98	L5	T6
6	55	I/O	66	97	K6	V7

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA
6	56	I/O	-	96	-	P7
6	57	I/O	-	94	-	V6
6	58	I/O	65	93	J6	T7
-	59	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	60	I/O	64	92	L6	P8
6	61	I/O	63	91	-	R8
6	62	I/O	62	89	-	M9
6	63	I/O	-	88	-	R10
6	64	I/O	-	87	-	V8
6	65	I/O	60	85	H6	N9
6	66	I/O	59	84	-	N8
-	67	CONF_DONE (6)	58	83	M3	U8
-	68	nSTATUS (6)	57	82	M4	U9
5	69	FAST4	56	81	M5	T9
-	70	GNDINT	GND	GND	GND	GND
-	71	GNDINT	-	-	-	-
-	72	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
-	73	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
-	74	GNDINT	-	-	-	-
-	75	GNDINT	GND	GND	GND	GND
-	76	GNDIO	GND	GND	GND	GND
5	77	FAST3	53	77	M8	T10
-	78	TCK (6)	52	76	M9	U10
-	79	TMS (6)	51	75	M10	U11
5	80	I/O	50	74	L7	V9
5	81	I/O	-	73	L8	P10
5	82	I/O	49	72	K7	T11
5	83	I/O	48	71	K8	P11
5	84	I/O	47	70	J8	R11
5	85	I/O	-	69	J7	V12
5	86	I/O	46	68	H8	M10
-	87	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5
5	88	I/O	-	66	-	T12
5	89	I/O	44	65	L9	R12
5	90	I/O	-	63	-	N11
5	91	I/O	43	62	K9	V13
5	92	I/O	41	61	H7	P12
5	93	I/O	-	60	K10	V14
5	94	I/O	-	59	L10	T13
5	95	I/O	40	58	-	U14
-	96	GNDIO	GND	GND	GND	GND
5	97	I/O	39	57	-	R13
5	98	I/O	38	56	-	R14
5	99	I/O	37	54	-	T15
-	100	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5
-	101	GNDIO	GND	GND	GND	GND
4	102	I/O	35	50	L11	R18
4	103	I/O	33	48	L12	N16
-	104	GNDINT	GND	GND	GND	GND
4	105	I/O	32	47	K11	L13
4	106	I/O	31	45	J11	N17
4	107	I/O	30	41	J10	L14
-	108	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	109	I/O	29	40	H11	M16
4	110	I/O	27	37	H10	P18
4	111	I/O	-	36	-	L15
4	112	I/O	26	35	-	K14

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA
-	113	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	114	I/O	25	34	J9	J13
4	115	I/O	24	33	-	M17
4	116	I/O, CLK3n (5)	-	32	H9	H16
4	117	CLK3p	23	31	G8	H15
4	118	I/O, CLK1n (5)	-	30	G11	K15
-	119	GNDIO	GND	GND	GND	GND
-	120	nCONFIG (6)	22	29	G10	K17
-	121	CLKLK_ENA (6), (10)	21	28	G9	K12
4	122	CLK1p	20	27	F9	K16
-	123	MSEL1 (6)	19	26	F10	J16
-	124	MSEL0 (6)	18	25	F11	J17
3	125	I/O	15	22	C11	L17
3	126	I/O	14	20	-	L16
3	127	I/O	-	19	E8	K18
3	128	I/O	13	18	-	J14
-	129	GNDINT	GND	GND	GND	GND
3	130	I/O	11	17	F8	J15
3	131	I/O	10	14	F7	G16
3	132	I/O	-	13	-	H13
3	133	I/O	9	12	C10	M18
-	134	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	135	I/O	8	11	E11	H14
3	136	I/O	-	9	E10	H17
3	137	I/O	7	7	E9	H18
3	138	I/O	6	5	D10	G18
-	139	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	140	I/O	3	4	D11	G17
3	141	I/O	2	2	C12	G14
-	142	GNDIO	GND	GND	GND	GND
2	143	I/O	143	207	B11	B15
2	144	I/O	142	206	C6	A15
2	145	I/O	141	205	B10	D14
2	146	I/O	140	204	D9	C14
-	147	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2
2	148	I/O	139	203	C9	A14
2	149	I/O	138	202	D8	A13
2	150	I/O	-	201	-	B13
2	151	I/O	137	200	C8	C13
2	152	I/O	-	198	-	D13
2	153	I/O	136	197	B9	E13
2	154	I/O	135	196	D7	C12
-	155	GNDIO	GND	GND	GND	GND
2	156	I/O	133	194	C7	A11
2	157	I/O	-	193	-	B11
2	158	I/O	132	192	B8	A10
2	159	I/O	-	191	-	A9
2	160	I/O	-	190	-	G10
2	161	I/O	131	188	B7	C11
2	162	I/O	130	187	E7	E12
-	163	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2
-	164	TRST (6)	129	186	A10	B10
-	165	NCEO (6)	128	185	A9	C10
1	166	FAST1	127	184	A8	D10
-	167	GNDINT	GND	GND	GND	GND
-	168	GNDINT	-	-	-	-

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA
-	169	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
-	170	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
-	171	GNDINT	GND	GND	GND	GND
-	172	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	173	FAST2	124	181	A5	B9
-	174	TDO (6)	123	180	A4	C9
-	175	GNDINT	-	-	-	GND
1	176	I/O	122	179	-	D9
1	177	I/O, INITDONE (4)	121	178	D6	E11
1	178	I/O, RDYnBSY (2)	120	177	E6	E10
1	179	I/O, CLKUSR (2)	119	176	F6	F10
1	180	I/O	118	175	B5	A7
1	181	I/O, DATA1 (2)	117	173	C5	F9
1	182	I/O	-	171	-	D8
-	183	GNDIO	GND	GND	GND	GND
1	184	I/O, DATA2 (2)	115	168	D5	E8
1	185	I/O	-	167	-	B7
1	186	I/O	114	166	B6	C8
1	187	I/O	113	164	B4	A5
1	188	I/O, DATA3 (2)	112	163	C4	B6
1	189	I/O	-	162	E5	F8
1	190	I/O	-	161	-	D7
-	191	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	192	I/O, DATA4 (2)	111	160	C3	C5
1	193	I/O	-	159	-	A4
1	194	I/O	110	158	A3	B4
1	195	I/O, DATA5 (2)	109	157	B3	B2
-	196	GNDIO	GND	GND	GND	GND
-	197	-	-	-	-	-

Pin Name	144-Pin TQFP	208-Pin PQFP	144-Pin FineLine BGA	324-Pin FineLine BGA
MSEL0 (6)	18	25	F11	J17
MSEL1 (6)	19	26	F10	J16
NSTATUS (6)	57	82	M4	U9
NCONFIG (6)	22	29	G10	K17
DCLK (6)	93	132	G2	J3
CONF_DONE (6)	58	83	M3	U8
INIT_DONE (4)	121	178	D6	E11
nCE (6)	91	130	H5	K2
nCEO (6)	128	185	A9	C10
nWS (2)	103	145	C2	K5
nRS (2)	102	142	D2	J6
nCS (2)	101	141	D3	H5
CS (2)	98	138	E3	M2
RDYnBSY (2)	120	177	E6	E10
CLKUSR (2)	119	176	F6	F10
DATA7 (2)	104	146	C1	H6
DATA6 (2)	105	150	B2	G4
DATA5 (2)	109	157	B3	B2
DATA4 (2)	111	160	C3	C5
DATA3 (2)	112	163	C4	B6
DATA2 (2)	115	168	D5	E8
DATA1 (2)	117	173	C5	F9
DATA0 (6), (7)	94	133	G3	J2
TDI (6)	90	129	H2	K3
TDO (6)	123	180	A4	C9
TCK (6)	52	76	M9	U10
TMS (6)	51	75	M10	U11
TRST (6)	129	186	A10	B10
Dedicated Fast I/Os	53, 56, 124, 127	77, 81, 181, 184	A5, A8, M5, M8	D10, B9, T10, T9
CLK1p	20	27	F9	K16
CLK2p	92	131	G7	J4
CLK3p	23	31	G8	H15
CLK4p	95	134	F2	L2
LOCK2 (9)	80	119	K3	N2
LOCK4 (9)	78	116	L2	R3
CLKLK_ENA (6), (10)	21	28	G9	K12
CLKLK_OUT2p (11)	81	120	J2	M3
CLKLK_FB2p	96	135	F4	N4
DEV_CLRn (4)	97	137	E4	L5
DEV_OE (4)	84	124	J3	L4
VCCINT	1, 16, 36, 55, 73, 86, 108, 125	1, 23, 52, 79, 105, 126, 156, 182	A7, B1, B12, F1, F12, H1, H12, M7	G6, G11, F7, H9, H12, J8, K11, L7, L10, M8, M13, N5, N12
VCCIO8	107	136	D1	F5, H7
VCCIO7	89	115	K1	K8, M6
VCCIO6	61	86	M2	L9, N7, P6
VCCIO5	45	53, 80	M11	M11, P13
VCCIO4	28	42	K12	L12, N14

Pin Name	144-Pin TQFP	208-Pin PQFP	144-Pin FineLine BGA	324-Pin FineLine BGA
VCCIO3	5	8	D12	J11, G13
VCCIO2	144	189, 208	A11	F12, H10
VCCIO1	116	172	A2	E6, G8
VCC_CKLK2 (3)	85	125	G6	J7
VCC_CKLK4 (3)	100	140	D4	K6
VCC_CKOUT2 (8)	83	123	H4	P3
GND	4, 12, 17, 34, 42, 54, 72, 74, 77, 87,106, 126, 134	10, 16, 24, 39, 43, 64, 78, 95, 114, 118, 127, 143, 149, 169, 183, 199	A1, A6, A12, E1, E12, G1, G12, J1, J12, M1, M6, M12	D4, D15, E5, E14, F6, F13, G7, G9, G12, H8, H11, J9, J10, K9, K10, L8, L11, M7, M12, N6, N13, P5, P14, R4, R15
GND_CKLK2 (3)	88	128	G5	K7
GND_CKLK4 (3)	99	139	E2	L6
GND_CKOUT2 (8)	82	122	H3	P2
No Connect (N.C.)	-	3, 6, 15, 21, 38, 44, 46, 49, 51, 55, 67, 90, 106, 107, 144, 147, 148, 151, 152, 153, 154, 155, 165, 170, 174, 195	-	A1, A12, A16, A17, A18, A2, A3, A6, A8, B1, B12, B14, B16, B17, B18, B3, B5, B8, C1, C15, C16, C17, C18, C2, C3, C4, C6, C7, D1, D11, D12, D16, D17, D18, D2, D3, D5, D6, E1, E15, E16, E17, E18, E2, E3, E4, E7, E9, F1, F11, F14, F15, F16, F17, F18, F2, F3, F4, G15, G2, G3, J1, J12, J18, K13, K4, L1, L18, M1, M14, M15, M5, N1, N10, N15, N18, P1, P15, P16, P17, P4, P9, R1, R16, R17, R2, R7, R9, T1, T14, T16, T17, T18, T2, T3, T5, T8, U1, U12, U13, U15, U16, U17, U18, U2, U3, U6, U7, V1, V10, V11, V15, V16, V17, V18, V2, V3, V4
Total User I/O Pins (12)	92	125	93	128

Notes:

(1) For the 144-pin and 208-pin QFP packages, four unique VCCIO levels are supported. The VCCIO pins for I/O banks 1 and 8 must be at the same level. The VCCIO pins for banks 6 and 7 form a single I/O bank. The VCCIO pins for I/O banks 4 and 5 must be at the same level. The VCCIO pins for I/O banks 2 and 3 must be at the same level. However, unique VREF settings are supported for each of the eight I/O banks.

(2) This pin can be used as a user I/O pin after configuration.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(6) This pin is a dedicated pin; it is not available as a user I/O pin.

(7) This pin is tri-stated in user mode.

(8) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(11) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(12) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.