I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
8	1	I/O	F6	E5
8	2	I/O	F5	E3
8	3	I/O	F4	F5
8	4	I/O	C1	F4
–	5	VCCINT	VCCINT	VCCINT
–	6	GNDINT	GND	GND
8	7	I/O	D1	E4
8	8	I/O	E2	F3
8	9	I/O	G6	D5
8	10	I/O	G5	G5
8	11	I/O	G4	G3
–	12	VCCIO	VCCIO8	VCCIO8
8	13	I/O	G3	G8
8	14	I/O	F2	G4
8	15	I/O	E1	C4
8	16	I/O	G2	G6
8	17	I/O	H6	H5
–	18	VCCINT	VCCINT	VCCINT
–	19	GNDINT	GND	GND
8	20	I/O	H4	G7
8	21	I/O	H3	H7
8	22	I/O	F1	H4
8	23	I/O	H2	H6
8	24	I/O	G1	K7
–	25	GNDIO	GND	GND
8	26	I/O	J6	J5
8	27	I/O	J5	H9
8	28	I/O	J4	J8
8	29	I/O	J3	H3
8	30	I/O	J2	K3
–	31	VCCINT	VCCINT	VCCINT
–	32	GNDINT	GND	GND
8	33	I/O	J1	J4
8	34	I/O	K6	K5
8	35	I/O	K5	J6
8	36	I/O	K4	L6
8	37	I/O	K3	J7
–	38	VCCIO	VCCIO8	VCCIO8
8	39	I/O	K2	J3
8	40	I/O	K1	K8
8	41	I/O, DATA6 (1)	L6	L8
8	42	I/O	L5	K6
8	43	I/O	L4	K4
–	44	VCCINT	VCCINT	VCCINT
–	45	GNDINT	GND	GND
8	46	I/O	L2	N5
8	47	I/O	L1	M8
8	48	I/O, DATA7 (1)	M6	M10

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
8	49	I/O	M5	M6
8	50	I/O	M4	L7
–	51	GNDIO	GND	GND
8	52	I/O	M3	L9
8	53	I/O	M2	M7
8	54	I/O, nWS (1)	M1	P9
8	55	I/O	N6	L5
8	56	I/O	N5	P8
–	57	VCCINT	VCCINT	VCCINT
–	58	GNDINT	GND	GND
8	59	I/O	N3	L4
8	60	I/O	N2	L3
8	61	I/O, nRS (1)	N1	N10
8	62	I/O	P6	R4
8	63	I/O	P5	M5
–	64	VCCIO	VCCIO8	VCCIO8
8	65	I/O	P4	M3
8	66	I/O	P3	P4
8	67	I/O, nCS (1)	P2	M9
8	68	I/O	P1	R3
8	69	I/O	R6	P5
–	70	VCCINT	VCCINT	VCCINT
–	71	GNDINT	GND	GND
–	72	VCC_CKLK4 (2)	R4	P10
–	73	GND_CKLK4 (2)	R3	R10
–	74	GND_CKLK4 (2)	R3	R10
8	75	I/O, CS (1)	R2	T6
8	76	I/O	R1	M4
8	77	I/O, DEV_CLRn (3)	T6	R9
–	78	VCCIO	VCCIO8	–
–	79	GNDIO	GND	GND
8	80	I/O, CLKLK_FB2n (4)	T5	T8
8	81	CLKLK_FB2p	T4	U8
8	82	I/O, CLK4n (4)	T3	R7
8	83	CLK4p	T2	R6
8	84	I/O, CLK2n (4)	T1	N9
–	85	VCCINT	VCCINT	VCCINT
–	86	GNDINT	GND	GND
–	87	DATA0 (5), (6)	U4	N6
–	88	DCLK (5)	U3	N7
8	89	CLK2p	U2	N8
–	90	nCE (5)	U1	P6
–	91	TDI (5)	W1	P7
–	92	VCCIO	VCCIO7	VCCIO7
–	93	GND_CKLK2 (2)	W2	P11
–	94	GND_CKLK2 (2)	W2	P11
–	95	GNDINT	GND	GND
–	96	VCCINT	VCCINT	VCCINT

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	97	VCC_CKLK2 (2)	W4	N11
7	98	I/O, DEV_OE (3)	Y5	R8
–	99	VCC_CKOUT2 (7)	Y1	V7
–	100	GND_CKOUT2 (7)	Y2	V6
–	101	CLKLK_OUT2p (8)	Y3	T7
7	102	I/O, CLKLK_OUT2n (4)	Y4	U7
–	103	VCCIO	VCCIO7	VCCIO7
7	104	I/O, LVDSTXINCLK1p	W5	D1
7	105	I/O, LVDSTXINCLK1n (4)	Y6	D2
7	106	I/O, LOCK2 (9)	AB6	U6
7	107	I/O, LVDSTXOUTCLK1n (4)	AA2	E1
7	108	I/O, LVDSTXOUTCLK1p	AA3	E2
–	109	GNDINT	GND	GND
–	110	VCCINT	VCCINT	VCCINT
7	111	I/O, LVDSTX01p	AA5	F1
7	112	I/O, LVDSTX01n (4)	AA6	F2
7	113	I/O	AB1	R5
7	114	I/O, LVDSTX02n (4)	AB2	G1
7	115	I/O, LVDSTX02p	AB3	G2
–	116	GNDIO	GND	GND
7	117	I/O, LVDSTX03p	AB4	H1
7	118	I/O, LVDSTX03n (4)	AB5	H2
7	119	I/O	AA1	T5
7	120	I/O, LVDSTX04n (4)	AC1	J1
7	121	I/O, LVDSTX04p	AC2	J2
–	122	GNDINT	GND	GND
–	123	VCCINT	VCCINT	VCCINT
7	124	I/O, LVDSTX05p	AC4	K1
7	125	I/O, LVDSTX05n (4)	AC5	K2
7	126	I/O, LOCK4 (9)	AC6	W7
7	127	I/O, LVDSTX06n (4)	AD1	L1
7	128	I/O, LVDSTX06p	AD2	L2
–	129	VCCIO	VCCIO7	VCCIO7
7	130	I/O, LVDSTX07p	AD3	M1
7	131	I/O, LVDSTX07n (4)	AD4	M2
7	132	I/O	AD5	T3
7	133	I/O, LVDSTX08n (4)	AD6	R1
7	134	I/O, LVDSTX08p	AE1	R2
–	135	GNDINT	GND	GND
–	136	VCCINT	VCCINT	VCCINT
7	137	I/O, LVDSTX09p	AE3	T1
7	138	I/O, LVDSTX09n (4)	AE4	T2
7	139	I/O	AE5	U5

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
7	140	I/O, LVDSTX10n (4)	AE6	U1
7	141	I/O, LVDSTX10p	AF1	U2
–	142	GNDIO	GND	GND
7	143	I/O, LVDSTX11p	AF2	V1
7	144	I/O, LVDSTX11n (4)	AF3	V2
7	145	I/O	AF4	T4
7	146	I/O, LVDSTX12n (4)	AF5	W1
7	147	I/O, LVDSTX12p	AF6	W2
–	148	GNDINT	GND	GND
–	149	VCCINT	VCCINT	VCCINT
7	150	I/O, LVDSTX13p	AH1	Y1
7	151	I/O, LVDSTX13n (4)	AG2	Y2
7	152	I/O	AG3	U4
7	153	I/O, LVDSTX14n (4)	AG4	AA1
7	154	I/O, LVDSTX14p	AG5	AA2
–	155	VCCIO	VCCIO7	VCCIO7
7	156	I/O, LVDSTX15p	AG6	AB1
7	157	I/O, LVDSTX15n (4)	AJ1	AB2
7	158	I/O	AH2	W4
7	159	I/O, LVDSTX16n (4)	AK1	AC1
7	160	I/O, LVDSTX16p	AH3	AC2
–	161	GNDINT	GND	GND
–	162	VCCINT	VCCINT	VCCINT
7	163	I/O	AH5	U3
7	164	I/O	AH6	V3
7	165	I/O	AJ2	W5
7	166	I/O	AL1	W6
7	167	I/O	AK2	V5
–	168	GNDIO	GND	GND
7	169	I/O	AJ3	V4
7	170	I/O	AJ4	W3
7	171	I/O	AJ5	Y5
7	172	I/O	AJ6	AB5
7	173	I/O	AM1	AA5
–	174	GNDINT	GND	GND
–	175	VCCINT	VCCINT	VCCINT
7	176	I/O	AK3	Y6
7	177	I/O	AK4	AA6
7	178	I/O	AK5	AA7
7	179	I/O	AK6	AB6
–	180	VCCIO	VCCIO7	VCCIO7
–	181	VCCIO	VCCIO6	VCCIO6
6	182	I/O	AL7	AB4
6	183	I/O	AM6	AA4
6	184	I/O	AP3	AC5
6	185	I/O	AN5	Y4
6	186	I/O	AR2	AE4
6	187	I/O	AP4	AB3

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
6	188	I/O	AL8	AF4
6	189	I/O	AM7	Y3
6	190	I/O	AN6	AD4
6	191	I/O	AR3	AA3
–	192	GNDIO	GND	GND
6	193	I/O	AP5	AE5
6	194	I/O	AL9	AD5
6	195	I/O	AR4	AD6
6	196	I/O	AM8	AB7
6	197	I/O	AN7	Y7
6	198	I/O	AP6	AC6
6	199	I/O	AR5	AB8
6	200	I/O	AM9	AF5
6	201	I/O	AL10	V8
6	202	I/O	AN8	AC7
–	203	VCCIO	VCCIO6	VCCIO6
6	204	I/O	AP7	AD7
6	205	I/O	AR6	T9
6	206	I/O	AM10	AE7
6	207	I/O	AN9	AA9
6	208	I/O	AL11	AF7
6	209	I/O	AP8	AA8
6	210	I/O	AR7	AC8
6	211	I/O	AM11	Y8
6	212	I/O	AN10	AD8
6	213	I/O	AP9	Y9
–	214	GNDIO	GND	GND
–	215	VCCINT	VCCINT	VCCINT
–	216	VCCINT	VCCINT	VCCINT
–	217	GNDINT	GND	GND
–	218	GNDINT	GND	GND
6	219	I/O	AR8	W9
6	220	I/O	AN11	AB9
6	221	I/O	AP10	W10
6	222	I/O	AR9	AC9
6	223	I/O	AL13	Y10
6	224	I/O	AM13	AD9
6	225	I/O	AN12	AA10
6	226	I/O	AP11	AB11
6	227	I/O	AL14	V11
6	228	I/O	AR10	AB10
–	229	VCCIO	VCCIO6	VCCIO6
6	230	I/O	AN13	AC10
6	231	I/O	AP12	AA11
6	232	I/O	AM14	AE9
6	233	I/O	AR11	Y11
6	234	I/O	AL15	AF9
6	235	I/O	AN14	W11

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
6	236	I/O	AP13	AF11
6	237	I/O	AR12	V12
6	238	I/O	AR13	AE10
6	239	I/O	AM15	W12
–	240	GNDIO	GND	GND
6	241	I/O	AN15	Y12
6	242	I/O	AL16	T13
–	243	VCCIO	VCCIO6	VCCIO6
6	244	I/O	AP14	W14
6	245	I/O	AR14	AB12
6	246	I/O	AP15	AF10
6	247	I/O	AR15	U13
6	248	I/O, LVDSDESKEW	AM16	U12
6	249	I/O	AN16	W13
6	250	I/O	AP16	AE11
6	251	I/O	AR16	V13
–	252	CONF_DONE (5)	AM17	AA12
–	253	nSTATUS (5)	AN17	AA13
5	254	FAST4	AP17	Y13
–	255	VCCIO	VCCIO5	VCCIO5
–	256	VCCINT	VCCINT	VCCINT
–	257	VCCINT	VCCINT	VCCINT
–	258	GNDINT	GND	GND
–	259	GNDINT	GND	GND
5	260	FAST3	AP19	Y14
–	261	TCK (5)	AN19	AA14
–	262	TMS (5)	AM19	AA15
5	263	I/O	AR20	AC13
5	264	I/O	AP20	AD17
5	265	I/O	AN20	AC12
5	266	I/O	AM20	AC14
5	267	I/O	AR21	AD10
5	268	I/O	AP21	AB13
5	269	I/O	AR22	V14
5	270	I/O	AP22	AB14
5	271	I/O	AL20	Y15
5	272	I/O	AN21	AC11
–	273	GNDIO	GND	GND
5	274	I/O	AM21	AD18
5	275	I/O	AR23	U14
5	276	I/O	AR24	AC15
5	277	I/O	AP23	V15
5	278	I/O	AN22	AB15
5	279	I/O	AL21	W15
5	280	I/O	AR25	AB16
5	281	I/O	AM22	T14
5	282	I/O	AP24	AD19
5	283	I/O	AN23	AA16

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	284	VCCIO	VCCIO5	VCCIO5
5	285	I/O	AR26	Y16
5	286	I/O	AL22	AC16
5	287	I/O	AP25	W16
5	288	I/O	AN24	AC17
5	289	I/O	AM23	U15
5	290	I/O	AL23	AB17
5	291	I/O	AR27	V16
5	292	I/O	AP26	AE16
5	293	I/O	AN25	AA17
5	294	I/O	AR28	AD20
–	295	VCCINT	VCCINT	VCCINT
–	296	VCCINT	VCCINT	VCCINT
–	297	GNDINT	GND	GND
–	298	GNDINT	GND	GND
–	299	GNDIO	GND	GND
5	300	I/O	AP27	AB18
5	301	I/O	AN26	Y17
5	302	I/O	AM25	AF16
5	303	I/O	AR29	AA18
5	304	I/O	AP28	AC18
5	305	I/O	AL25	W17
5	306	I/O	AN27	AE17
5	307	I/O	AM26	Y18
5	308	I/O	AR30	AF17
5	309	I/O	AP29	W18
–	310	VCCIO	VCCIO5	VCCIO5
5	311	I/O	AN28	AA19
5	312	I/O	AL26	AD21
5	313	I/O	AM27	Y19
5	314	I/O	AR31	AD22
5	315	I/O	AP30	W20
5	316	I/O	AN29	AC19
5	317	I/O	AM28	Y20
5	318	I/O	AR32	AB20
5	319	I/O	AL27	AB19
5	320	I/O	AP31	AC20
–	321	GNDIO	GND	GND
5	322	I/O	AR33	AD23
5	323	I/O	AN30	AA20
5	324	I/O	AM29	AB24
5	325	I/O	AL28	AC22
5	326	I/O	AP32	AC21
5	327	I/O	AR34	Y23
5	328	I/O	AN31	Y24
5	329	I/O	AP33	AA23
5	330	I/O	AM30	AA24
5	331	I/O	AL29	AB23

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	332	VCCIO	VCCIO5	VCCIO5
–	333	VCCIO	VCCIO4	VCCIO4
4	334	I/O	AL33	AA21
4	335	I/O	AK30	Y22
4	336	I/O	AK31	AB21
4	337	I/O	AK32	U19
–	338	VCCINT	VCCINT	VCCINT
–	339	GNDINT	GND	GND
4	340	I/O	AL34	AB22
4	341	I/O	AM35	V19
4	342	I/O	AJ30	T18
4	343	I/O	AJ31	W21
4	344	I/O	AJ32	V20
–	345	GNDIO	GND	GND
4	346	I/O	AJ33	V21
4	347	I/O	AK34	Y21
4	348	I/O	AL35	W22
4	349	I/O	AJ34	AA22
4	350	I/O	AH30	U20
–	351	VCCINT	VCCINT	VCCINT
–	352	GNDINT	GND	GND
4	353	I/O	AH32	R17
4	354	I/O	AH33	W23
4	355	I/O	AK35	T19
4	356	I/O	AH34	U21
4	357	I/O	AJ35	P17
–	358	VCCIO	VCCIO4	VCCIO4
4	359	I/O	AG30	R18
4	360	I/O	AG31	W24
4	361	I/O	AG32	T20
4	362	I/O	AG33	V24
4	363	I/O	AG34	N16
–	364	VCCINT	VCCINT	VCCINT
–	365	GNDINT	GND	GND
4	366	I/O	AG35	V22
4	367	I/O	AF30	R19
4	368	I/O	AF31	V23
4	369	I/O	AF32	P18
4	370	I/O	AF33	N17
–	371	GNDIO	GND	GND
4	372	I/O	AF34	T21
4	373	I/O	AF35	R21
4	374	I/O	AE30	U22
4	375	I/O	AE31	R20
4	376	I/O	AE32	P22
–	377	VCCINT	VCCINT	VCCINT
–	378	GNDINT	GND	GND
4	379	I/O	AE34	N18

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
4	380	I/O	AE35	U23
4	381	I/O	AD30	N19
4	382	I/O	AD31	N22
4	383	I/O	AD32	L20
–	384	VCCIO	VCCIO4	VCCIO4
4	385	I/O	AD33	M17
4	386	I/O	AD34	T22
4	387	I/O	AD35	M18
4	388	I/O	AC30	T23
4	389	I/O	AC31	R23
–	390	VCCINT	VCCINT	VCCINT
–	391	GNDINT	GND	GND
4	392	I/O	AC33	U24
4	393	I/O	AC34	R24
4	394	I/O	AC35	T24
4	395	I/O	AB30	M21
4	396	I/O	AB31	M24
–	397	GNDIO	GND	GND
4	398	I/O	AB32	M22
4	399	I/O	AB33	R22
4	400	I/O	AB34	M23
4	401	I/O	AB35	L22
4	402	I/O, LOCK1 (9)	AA30	L21
–	403	VCCINT	VCCINT	VCCINT
–	404	GNDINT	GND	GND
4	405	I/O	AA32	L23
4	406	I/O	AA33	L24
4	407	I/O	AA34	N23
–	408	VCC_CKLK1 (2)	AA35	AF18
–	409	GND_CKLK1 (2)	Y30	AE18
–	410	GND_CKLK1 (2)	Y30	AE18
–	411	VCCIO	VCCIO4	VCCIO4
4	412	I/O, CLKLK_FB1n (4)	Y31	AF20
4	413	CLKLK_FB1p	Y32	AE20
4	414	I/O, CLK3n (4)	Y33	M20
4	415	CLK3p	Y34	M19
4	416	I/O, CLK1n (4)	Y35	P19
–	417	VCCINT	VCCINT	VCCINT
–	418	GNDINT	GND	GND
–	419	VCCIO	VCCIO4	VCCIO4
–	420	nCONFIG (5)	W32	P21
–	421	CLKLK_ENA (5), (10)	W33	P16
4	422	CLK1p	W34	P20
–	423	MSEL1 (5)	W35	N20
–	424	MSEL0 (5)	U35	N21
–	425	GNDINT	GND	GND
–	426	VCCINT	VCCINT	VCCINT
–	427	VCC_CKOUT1 (7)	U33	AF22

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	428	GND_CKOUT1 (7)	U32	AE22
–	429	CLKLK_OUT1p (8)	U31	AE23
3	430	I/O, CLKLK_OUT1n (4)	T35	AF23
–	431	VCC_CKLK3 (2)	T34	AC26
–	432	GNDIO	GND	GND
–	433	GND_CKLK3 (2)	V35	N25
–	434	GND_CKLK3 (2)	T33	AC25
3	435	I/O, LVDSRXINCLK1p	T32	AB25
3	436	I/O, LVDSRXINCLK1n (4)	T31	AB26
3	437	I/O	T30	J23
3	438	I/O	R35	L19
–	439	GNDINT	GND	GND
–	440	VCCINT	VCCINT	VCCINT
3	441	I/O, LVDSRX01p	R33	AA25
3	442	I/O, LVDSRX01n (4)	R32	AA26
3	443	I/O, LOCK3 (9)	R31	L18
3	444	I/O, LVDSRX02n (4)	R30	Y25
3	445	I/O, LVDSRX02p	P35	Y26
–	446	VCCIO	VCCIO3	VCCIO3
3	447	I/O, LVDSRX03p	P34	W25
3	448	I/O, LVDSRX03n (4)	P33	W26
3	449	I/O	P32	J24
3	450	I/O, LVDSRX04n (4)	P31	V25
3	451	I/O, LVDSRX04p	P30	V26
–	452	GNDINT	GND	GND
–	453	VCCINT	VCCINT	VCCINT
3	454	I/O, LVDSRX05p	N34	U25
3	455	I/O, LVDSRX05n (4)	N33	U26
3	456	I/O	N32	K21
3	457	I/O, LVDSRX06n (4)	N31	T25
3	458	I/O, LVDSRX06p	N30	T26
–	459	GNDIO	GND	GND
3	460	I/O, LVDSRX07p	M35	R25
3	461	I/O, LVDSRX07n (4)	M34	R26
3	462	I/O	M33	K23
3	463	I/O, LVDSRX08n (4)	M32	M25
3	464	I/O, LVDSRX08p	M31	M26
–	465	GNDINT	GND	GND
–	466	VCCINT	VCCINT	VCCINT
3	467	I/O, LVDSRX09p	L35	L25
3	468	I/O, LVDSRX09n (4)	L34	L26
3	469	I/O	L33	K20
3	470	I/O, LVDSRX10n (4)	L32	K25
3	471	I/O, LVDSRX10p	L31	K26
–	472	VCCIO	VCCIO3	VCCIO3
3	473	I/O, LVDSRX11p	L30	J25

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
3	474	I/O, LVDSRX11n (4)	K35	J26
3	475	I/O	K34	K22
3	476	I/O, LVDSRX12n (4)	K33	H25
3	477	I/O, LVDSRX12p	K32	H26
–	478	GNDINT	GND	GND
–	479	VCCINT	VCCINT	VCCINT
3	480	I/O, LVDSRX13p	K30	G25
3	481	I/O, LVDSRX13n (4)	J35	G26
3	482	I/O	H35	K24
3	483	I/O, LVDSRX14n (4)	J34	F25
3	484	I/O, LVDSRX14p	J33	F26
–	485	GNDIO	GND	GND
3	486	I/O, LVDSRX15p	J32	E25
3	487	I/O, LVDSRX15n (4)	J31	E26
3	488	I/O	J30	H24
3	489	I/O, LVDSRX16n (4)	G35	D25
3	490	I/O, LVDSRX16p	H34	D26
–	491	GNDINT	GND	GND
–	492	VCCINT	VCCINT	VCCINT
3	493	I/O	H33	K19
3	494	I/O	H32	J20
3	495	I/O	H31	G22
3	496	I/O	H30	H20
3	497	I/O	G34	H22
–	498	VCCIO	VCCIO3	VCCIO3
3	499	I/O	E35	J22
3	500	I/O	F34	G24
3	501	I/O	G33	H21
3	502	I/O	G32	G21
3	503	I/O	G31	J21
–	504	GNDINT	GND	GND
–	505	VCCINT	VCCINT	VCCINT
3	506	I/O	D35	F22
3	507	I/O	E34	G20
3	508	I/O	F33	F21
3	509	I/O	F32	E22
–	510	VCCIO	VCCIO2	–
–	511	GNDIO	GND	GND
2	512	I/O	E29	E23
2	513	I/O	D30	D22
2	514	I/O	B33	F24
2	515	I/O	C31	E24
2	516	I/O	A34	H23
2	517	I/O	B32	C23
2	518	I/O	E28	G23
2	519	I/O	D29	C22
2	520	I/O	C30	F23
2	521	I/O	A33	B23

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	522	VCCIO	VCCIO2	VCCIO2
2	523	I/O	B31	A23
2	524	I/O	E27	E21
2	525	I/O	A32	B22
2	526	I/O	D28	F20
2	527	I/O	C29	D21
2	528	I/O	B30	C21
2	529	I/O	A31	E20
2	530	I/O	D27	J19
2	531	I/O	E26	A22
2	532	I/O	C28	G19
–	533	GNDIO	GND	GND
2	534	I/O	B29	F19
2	535	I/O	A30	E19
2	536	I/O	D26	K18
2	537	I/O	C27	D20
2	538	I/O	E25	H18
2	539	I/O	B28	C20
2	540	I/O	A29	G18
2	541	I/O	D25	D19
2	542	I/O	C26	E18
2	543	I/O	B27	B20
–	544	VCCIO	VCCIO2	VCCIO2
–	545	GNDINT	GND	GND
–	546	GNDINT	GND	GND
–	547	VCCINT	VCCINT	VCCINT
–	548	VCCINT	VCCINT	VCCINT
–	549	GNDINT	–	–
2	550	I/O	A28	A20
2	551	I/O	C25	F18
2	552	I/O	B26	C19
2	553	I/O	A27	E17
2	554	I/O	E23	D18
2	555	I/O	D23	F17
2	556	I/O	C24	C18
2	557	I/O	B25	G17
2	558	I/O	E22	B18
2	559	I/O	A26	H17
–	560	GNDIO	GND	GND
2	561	I/O	C23	F16
2	562	I/O	B24	D17
2	563	I/O	D22	J17
2	564	I/O	A25	E16
2	565	I/O	E21	G16
2	566	I/O	C22	A18
2	567	I/O	B23	H16
2	568	I/O	A24	C17
2	569	I/O	A23	E15

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
2	570	I/O	D21	D16
–	571	VCCIO	VCCIO2	VCCIO2
2	572	I/O	C21	B17
2	573	I/O	E20	F15
2	574	I/O	B22	A17
2	575	I/O	A22	E14
2	576	I/O	B21	H15
2	577	I/O	A21	E13
2	578	I/O	D20	L14
2	579	I/O	C20	G15
2	580	I/O	B20	K15
2	581	I/O	A20	J16
–	582	TRST (5)	D19	F14
–	583	nCEO (5)	C19	G14
1	584	FAST1	B19	H14
–	585	GNDINT	GND	GND
–	586	GNDINT	GND	GND
–	587	VCCINT	VCCINT	VCCINT
–	588	VCCINT	VCCINT	VCCINT
–	589	GNDIO	GND	GND
1	590	FAST2	B17	F13
–	591	TDO (5)	C17	G13
–	592	GNDINT	GND	GND
1	593	I/O	A16	D15
1	594	I/O	B16	D14
1	595	I/O, INITDONE (3)	C16	J15
1	596	I/O	D16	A12
1	597	I/O	A15	D13
1	598	I/O	B15	B11
1	599	I/O, RDYnBSY (1)	A14	J14
1	600	I/O	B14	B12
1	601	I/O	E16	H13
1	602	I/O, CLKUSR (1)	C15	K14
–	603	VCCIO	VCCIO1	VCCIO1
1	604	I/O	D15	F12
1	605	I/O	A13	A11
1	606	I/O	A12	E12
1	607	I/O	B13	A10
1	608	I/O	C14	D12
1	609	I/O	E15	D11
1	610	I/O	A11	E11
1	611	I/O	D14	B10
1	612	I/O	B12	C10
1	613	I/O, DATA1 (1)	C13	K13
–	614	GNDIO	GND	GND
1	615	I/O	A10	J13
1	616	I/O	E14	D10
–	617	VCCIO	VCCIO1	VCCIO1

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
1	618	I/O	B11	H12
1	619	I/O	C12	E10
1	620	I/O	D13	F11
1	621	I/O	E13	B9
1	622	I/O	A9	G12
1	623	I/O	B10	C9
1	624	I/O	C11	G11
1	625	I/O, DATA2 (1)	A8	J12
–	626	GNDINT	GND	GND
–	627	GNDINT	GND	GND
–	628	VCCINT	VCCINT	VCCINT
–	629	VCCINT	VCCINT	VCCINT
–	630	VCCIO	VCCIO1	VCCIO1
1	631	I/O	B9	E9
1	632	I/O	C10	F9
1	633	I/O	D11	D9
1	634	I/O	A7	K12
1	635	I/O	B8	A9
1	636	I/O	E11	H11
1	637	I/O	C9	D8
1	638	I/O	D10	E8
1	639	I/O	A6	C8
1	640	I/O, DATA3 (1)	B7	F10
–	641	GNDIO	GND	GND
1	642	I/O	C8	F8
1	643	I/O	E10	E7
1	644	I/O	D9	G10
1	645	I/O	A5	C7
1	646	I/O	B6	H10
1	647	I/O	C7	B7
1	648	I/O	D8	J11
1	649	I/O	A4	D7
1	650	I/O	E9	D6
1	651	I/O, DATA4 (1)	B5	G9
–	652	VCCIO	VCCIO1	VCCIO1
1	653	I/O	A3	A7
1	654	I/O	C6	F7
1	655	I/O	D7	E6
1	656	I/O	E8	C5
1	657	I/O	B4	C6
1	658	I/O	A2	B5
1	659	I/O	C5	A5
1	660	I/O	B3	B4
1	661	I/O	D6	A4
1	662	I/O, DATA5 (1)	E7	F6
–	663	GNDIO	GND	GND
–	664	–	–	–

Pin Name	652-Pin BGA	672-Pin FineLine BGA
MSEL0 (5)	U35	N21
MSEL1 (5)	W35	N20
nSTATUS (5)	AN17	AA13
nCONFIG (5)	W32	P21
DCLK (5)	U3	N7
CONF_DONE (5)	AM17	AA12
INIT_DONE (3)	C16	J15
nCE (5)	U1	P6
nCEO (5)	C19	G14
nWS (1)	M1	P9
nRS (1)	N1	N10
nCS (1)	P2	M9
CS (1)	R2	T6
RDYnBSY (1)	A14	J14
CLKUSR (1)	C15	K14
DATA7 (1)	M6	M10
DATA6 (1)	L6	L8
DATA5 (1)	E7	F6
DATA4 (1)	B5	G9
DATA3 (1)	B7	F10
DATA2 (1)	A8	J12
DATA1 (1)	C13	K13
DATA0 (5), (6)	U4	N6
TDI (5)	W1	P7
TDO (5)	C17	G13
TCK (5)	AN19	AA14
TMS (5)	AM19	AA15
TRST (5)	D19	F14
Dedicated Fast I/Os	AP19, AP17, B17, B19	Y14, Y13, F13, H14
CLK1p	W34	P20
CLK2p	U2	N8
CLK3p	Y34	M19
CLK4p	T2	R6
LOCK1 (9)	AA30	L21
LOCK2 (9)	AB6	U6
LOCK3 (9)	R31	L18
LOCK4 (9)	AC6	W7
CLKLK_ENA (5), (10)	W33	P16
CLKLK_OUT1p (8)	U31	AE23
CLKLK_OUT2p (8)	Y3	T7
CLKLK_FB1p	Y32	AE20
CLKLK_FB2p	T4	U8
DEV_CLRn (3)	T6	R9
DEV_OE (3)	Y5	R8

Pin Name	652-Pin BGA	672-Pin FineLine BGA
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24,C1, C2, C25, C26, D3, D24,K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25,AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO1	C4, D5, E17	A6, J10, L12
VCCIO2	E19, D31, C32	A13, K16, M14
VCCIO3	F30, F31, U30	A21, L17, N15
VCCIO4	W30, AL31, AL32	N24, R16, U18
VCCIO5	AN32, AN33, AL19	T15, V17, AF21
VCCIO6	AL17, AM5, AN4	R13, U11, V10, AF13
VCCIO7	AL3, AL4, W6	P12, T10, AF6
VCCIO8	U6, E3, E4	K9, M11, N3
VCC_CKLK1 (2)	AA35	AF18
VCC_CKLK2 (2)	W4	N11
VCC_CKLK3 (2)	T34	AC26
VCC_CKLK4 (2)	R4	P10
VCC_CKOUT1 (7)	U33	AF22
VCC_CKOUT2 (7)	Y1	V7
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D17, D18, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25
GND_CKLK1 (2)	Y30	AE18
GND_CKLK2 (2)	W2	P11
GND_CKLK3 (2)	T33, V35	AC25, N25
GND_CKLK4 (2)	R3	R10
GND_CKOUT1 (7)	U32	AE22
GND_CKOUT2 (7)	Y2	V6
No Connect (N.C.)		A15, A16, B13, B14, B15, B16, C11, C12, C14, C15, C16, AF12, AF15, AE12, AE13, AE14, AE15, AD11, AD12, AD14, AD15, AD16
Total User I/O Pins (11)	488	488

Notes:

(1) This pin can be used as a user I/O pin after configuration.

(2) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(4) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(5) This pin is a dedicated pin; it is not available as a user I/O pin.

(6) This pin is tri-stated in user mode.

(7) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(8) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.