I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
8	1	I/O	–	152	171	–	D5	F26
8	2	I/O	–	151	170	–	E3	H23
8	3	I/O, DATA6 (2)	105	150	169		G4	F24
8	4	I/O	–	148	168	–	F3	G25
–	5	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	6	I/O	–	147	167	–	G2	H25
8	7	I/O, DATA7 (2)	104	146	166	C1	H6	G23
8	8	I/O, nWS (2)	103	145	164	C2	K5	H22
8	9	I/O	–	144	163	–	F2	H26
8	10	I/O, nRS (2)	102	142	161	D2	J6	H24
–	11	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	12	I/O, nCS (2)	101	141	160	D3	H5	J24
–	13	VCC_CKLK4 (3)	100	140	159	D4	K6	K24
–	14	GND_CKLK4 (3)	99	139	158	E2	L6	L22
–	15	GND_CKLK4 (3)	99	139	158	E2	L6	L22
8	16	I/O, CS (2)	98	138	157	E3	M2	K25
8	17	I/O, DEV_CLRn (4)	97	137	156	E4	L5	L23
–	18	GNDINT	GND	GND	GND	GND	GND	GND
8	19	I/O, CLKLK_FB2n (5)	–	–	–	F5	M4	L24
8	20	CLKLK_FB2p	96	135	155	F4	N4	L25
8	21	I/O, CLK4n (5)	–	–	–	F3	L3	L26
8	22	CLK4p	95	134	154	F2	L2	M23
8	23	I/O, CLK2n (5)	–	–	–	G4	J5	M24
–	24	DATA0 (6), (7)	94	133	153	G3	J2	M26
–	25	DCLK(6)	93	132	152	G2	J3	N25
8	26	CLK2p	92	131	151	G7	J4	N26
–	27	nCE (6)	91	130	150	H5	K2	P26
–	28	TDI (6)	90	129	149	H2	K3	P25
–	29	GNDIO	GND	GND	GND	GND	GND	GND
–	30	GND_CKLK2 (3)	88	128	147	G5	K7	P24
–	31	GND_CKLK2 (3)	88	128	147	G5	K7	P24
–	32	VCC_CKLK2 (3)	85	125	144	G6	J7	P23
7	33	I/O, DEV_OE (4)	84	124	143	J3	L4	R26
–	34	VCC_CKOUT2 (8)	83	123	142	H4	P3	R25
–	35	GND_CKOUT2 (8)	82	122	141	H3	P2	R24
7	36	I/O, CLKLK_OUT2n (5)	–	121	140	K2	N3	R22

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
–	37	CLKLK_OUT2p (9)	81	120	139	J2	M3	R23
–	38	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	39	I/O, LOCK2 (10)	80	119	138	K3	N2	T24
7	40	I/O	79	117	136	J4	G3	T23
7	41	I/O, LOCK4 (10)	78	116	135	L2	R3	V25
7	42	I/O	–	113	134	–	H2	W24
7	43	I/O	–	112	133	–	H3	W23
–	44	VCCIO	VCCIO7	VCCIO7	_IR2	VCCIO7	VCCIO7	VCCIO7
7	45	I/O	–	111	131	–	H4	U26
7	46	I/O	–	–	130	–	G5	U25
7	47	I/O	–	110	129	–	G1	U24
7	48	I/O	–	–	128	–	K4	U23
7	49	I/O	76	109	127	L1	H1	U22
–	50	GNDINT	GND	GND	GND	GND	GND	GND
7	51	I/O	–	–	126	–	K1	V26
7	52	I/O	–	–	125	–	L1	V24
7	53	I/O	75	108	124	L3	M1	W26
7	54	I/O	–	107	123	–	N1	V23
–	55	GNDIO	GND	GND	GND	GND	GND	GND
–	56	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	57	I/O	–	106	–	–	T3	AD24
6	58	I/O	–	–	–	–	V3	AE25
6	59	I/O	–	–	–	–	V4	AD23
6	60	I/O	–	–	–	–	P4	AE24
6	61	I/O	–	–	–	–	M5	AF25
6	62	I/O	71	104	119	K4	T4	AF24
6	63	I/O	–	103	118	–	U4	AD22
6	64	I/O	70	102	117	J5	U5	AE23
6	65	I/O	–	–	–	–	T5	AF23
6	66	I/O	69	101	115	H6	R5	AE22
–	67	GNDIO	GND	GND	GND	GND	GND	GND
6	68	I/O	68	100	114	L4	V5	AD21
6	69	I/O	–	99	113	–	R6	AF22
6	70	I/O	67	98	112	K5	T6	AE21
6	71	I/O	–	–	–	–	U6	AD20
6	72	I/O	66	97	110	J6	V6	AF21
6	73	I/O	–	96	109	–	P7	AE20
6	74	I/O	–	94	107	–	V7	AD19
6	75	I/O	–	–	–	–	U7	AF20
6	76	I/O	65	93	105	L5	T7	AE19
6	77	I/O	–	–	–	–	R7	AD18
–	78	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	79	I/O	64	92	103	K6	N8	AF19
6	80	I/O	63	91	102	–	V8	AE18
6	81	I/O	–	90	101	–	P8	AF18

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
6	82	I/O	62	89	100	–	T8	AD17
6	83	I/O	–	88	99	–	R8	AE17
6	84	I/O	–	87	98	–	M9	AF17
6	85	I/O	60	85	96	L6	N9	AD16
6	86	I/O	59	84	95	–	P9	AE16
6	87	I/O	–	–	–	–	R9	AF16
6	88	I/O	–	–	–	–	R10	AD15
–	89	CONF_DONE (6)	58	83	93	M3	U8	AE15
–	90	nSTATUS (6)	57	82	92	M4	U9	AF15
5	91	FAST4	56	81	91	M5	T9	AE14
–	92	GNDINT	GND	GND	GND	GND	GND	GND
–	93	GNDINT	–	–	–	–	–	–
–	94	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	95	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	96	GNDINT	–	–	–	–	–	–
–	97	GNDINT	GND	GND	GND	GND	GND	GND
–	98	GNDIO	GND	GND	GND	GND	GND	GND
5	99	FAST3	53	77	88	M8	T10	AF12
–	100	TCK (6)	52	76	87	M9	U10	AE12
–	101	TMS (6)	51	75	86	M10	U11	AF11
5	102	I/O	50	74	85	L7	V9	AE11
5	103	I/O	–	73	84	–	P10	AD11
5	104	I/O	–	–	–	–	V10	AF10
5	105	I/O	49	72	82	K7	N10	AE10
5	106	I/O	–	–	–	–	R11	AD10
5	107	I/O	48	71	81	L8	P11	AF9
5	108	I/O	–	–	–	–	T11	AE9
5	109	I/O	47	70	79	J7	M10	AF8
5	110	I/O	–	69	77	–	V11	AD9
5	111	I/O	46	68	76	H7	N11	AE8
–	112	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
5	113	I/O	–	67	75	–	R12	AF7
5	114	I/O	–	66	74	–	T12	AD8
5	115	I/O	44	65	73	K8	P12	AE7
5	116	I/O	–	63	72	–	U12	AF6
5	117	I/O	43	62	71	L9	V12	AD7
5	118	I/O	41	61	70	J8	R13	AE6
5	119	I/O	–	–	–	–	T13	AF5
5	120	I/O	–	60	69	–	U13	AD6
5	121	I/O	–	59	68	–	V13	AE5
5	122	I/O	40	58	66	H8	R14	AF4
–	123	GNDIO	GND	GND	GND	GND	GND	GND
5	124	I/O	39	57	65	K9	T14	AF3
5	125	I/O	–	–	–	–	U14	AE4
5	126	I/O	38	56	63	L10	V14	AD5
5	127	I/O	–	55	62	–	T15	AF2

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
5	128	I/O	37	54	61	K10	U15	AE3
5	129	I/O	–	–	–	–	R16	AD4
5	130	I/O	–	–	–	–	V15	AC5
5	131	I/O	–	51	–	–	T16	AE2
5	132	I/O	–	–	–	–	U16	AD3
5	133	I/O	–	–	–	–	V16	AC4
–	134	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
–	135	GNDIO	GND	GND	GND	GND	GND	GND
4	136	I/O	35	50	53	L12	T17	V5
4	137	I/O	–	49	52	–	U18	W2
4	138	I/O	–	–	51	–	R18	V4
4	139	I/O	33	48	50	L11	P18	W1
–	140	GNDINT	GND	GND	GND	GND	GND	GND
4	141	I/O	32	47	49	K11	N17	V3
4	142	I/O	–	46	48	–	N16	U5
4	143	I/O	31	45	47	J9	K13	V2
4	144	I/O	–	44	46	–	M17	V1
4	145	I/O	30	41	44	J11	K14	U3
–	146	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	147	I/O	29	40	43	J10	M16	U2
4	148	I/O	–	38	41	–	M15	T5
4	149	I/O	27	37	40	H11	J13	U1
4	150	I/O	–	36	39	–	L13	T4
4	151	I/O	26	35	38	H10	J12	T3
–	152	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	153	I/O	25	34	37	–	L15	T2
4	154	I/O	24	33	36	–	L14	R5
4	155	I/O, CLK3n (5)	–	32	35	H9	H16	T1
4	156	CLK3p	23	31	34	G8	H15	R4
4	157	I/O, CLK1n (5)	–	30	–	G11	K15	R3
–	158	GNDIO	GND	GND	GND	GND	GND	GND
–	159	nCONFIG (6)	22	29	33	G10	K17	R1
–	160	CLKLK_ENA (6), (11)	21	28	32	G9	K12	P4
4	161	CLK1p	20	27	31	F9	K16	P3
–	162	MSEL1 (6)	19	26	30	F10	J16	P2
–	163	MSEL0 (6)	18	25	29	F11	J17	P1
3	164	I/O	15	22	25	F8	L17	N1
3	165	I/O	–	21	24	–	M18	N2
3	166	I/O	14	20	23	F7	K18	M1
3	167	I/O	–	19	22	–	N18	M2
3	168	I/O	13	18	21	E10	J18	M3
–	169	GNDINT	GND	GND	GND	GND	GND	GND
3	170	I/O	11	17	20	E11	J15	M4
3	171	I/O	–	15	18	–	H17	L2
3	172	I/O	10	14	17	E9	J14	L3
3	173	I/O	–	13	16	–	H18	K1

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
3	174	I/O	9	12	15	E8	G17	L4
–	175	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	176	I/O	8	11	14	D10	L18	K2
3	177	I/O	–	9	13	–	G18	L5
3	178	I/O	7	7	11	D11	G16	K3
3	179	I/O	–	6	10	–	F17	J1
3	180	I/O	6	5	9	C10	H14	K4
–	181	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	182	I/O	–	–	8	–	G15	J2
3	183	I/O	3	4	7	C11	L16	J3
3	184	I/O	–	–	6	–	H13	K5
3	185	I/O	2	3	5	C12	G14	H2
–	186	GNDIO	GND	GND	GND	GND	GND	GND
2	187	I/O	–	2	–	–	A17	C3
2	188	I/O	–	–	–	–	A16	B2
2	189	I/O	–	–	–	–	B16	D5
2	190	I/O	–	–	–	–	E15	C4
2	191	I/O	–	–	–	–	A15	B3
2	192	I/O	143	207	239	B11	B15	A2
2	193	I/O	142	206	238	D9	C15	C5
2	194	I/O	–	–	–	–	F14	B4
2	195	I/O	141	205	236	C9	A14	A3
2	196	I/O	140	204	235	B10	B14	A4
–	197	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2
2	198	I/O	139	203	234	D8	C14	B5
2	199	I/O	–	–	–	–	D14	C6
2	200	I/O	138	202	232	E7	A13	A5
2	201	I/O	–	201	231	–	B13	B6
2	202	I/O	137	200	230	B9	C13	C7
2	203	I/O	–	198	228	–	D13	A6
2	204	I/O	–	-	-	–	A12	B7
2	205	I/O	136	197	227	C6	E13	C8
2	206	I/O	–	–	–	–	B12	A7
2	207	I/O	135	196	225	C8	C12	B8
–	208	GNDIO	GND	GND	GND	GND	GND	GND
2	209	I/O	–	195	224	–	E12	C9
2	210	I/O	133	194	223	D7	D12	A8
2	211	I/O	–	193	222	–	A11	B9
2	212	I/O	132	192	221	C7	B11	A9
2	213	I/O	–	–	–	–	F11	C10
2	214	I/O	–	191	220	–	C11	B10
2	215	I/O	–	190	219	–	D11	A10
2	216	I/O	131	188	217	B8	A10	C11
2	217	I/O	–	–	–	–	G10	B11
2	218	I/O	130	187	215	B7	A9	A11
–	219	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2
–	220	TRST (6)	129	186	214	A10	B10	B12

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
–	221	NCEO	128	185	213	A9	C10	A12
1	222	FAST1	127	184	212	A8	D10	A13
–	223	GNDINT	GND	GND	GND	GND	GND	GND
–	224	GNDINT	–	–	–	–	–	–
–	225	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	226	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	227	GNDINT	GND	GND	GND	GND	GND	GND
–	228	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	229	FAST2	124	181	209	A5	B9	A15
–	230	TDO (6)	123	180	208	A4	C9	B15
–	231	GNDINT	GND	GND	GND	GND	GND	GND
1	232	I/O	122	179	207	B6	D9	C15
1	233	I/O, INITDONE (4)	121	178	206	D6	E11	A16
1	234	I/O, RDYnBSY (2)	120	177	205	E6	E10	B16
1	235	I/O, CLKUSR (2)	119	176	204	F6	F10	C16
1	236	I/O	–	–	–	–	E9	B17
1	237	I/O	118	175	202	B5	D8	C17
1	238	I/O	–	174	201	–	C8	A18
1	239	I/O, DATA1 (2)	117	173	200	C5	F9	B18
1	240	I/O	–	171	198	–	B8	A19
1	241	I/O	–	–	–	–	A8	A17
–	242	GNDIO	GND	GND	GND	GND	GND	GND
1	243	I/O	–	170	196	–	D7	C18
1	244	I/O, DATA2 (2)	115	168	195	D5	E8	B20
1	245	I/O	–	167	194	–	C7	B19
1	246	I/O	114	166	193	B4	B7	A20
1	247	I/O	–	165	192	–	A7	C19
1	248	I/O	113	164	191	E5	E7	A21
1	249	I/O	–	–	–	–	C6	C20
1	250	I/O, DATA3 (2)	112	163	189	C4	B6	B22
1	251	I/O	–	162	187	–	F8	B21
1	252	I/O	–	161	186	–	D6	A22
–	253	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	254	I/O, DATA4 (2)	111	160	185	C3	C5	A25
1	255	I/O	–	159	184	–	A6	C21
1	256	I/O	110	158	183	A3	B5	A23
1	257	I/O	–	–	–	–	A5	B23
1	258	I/O, DATA5 (2)	109	157	181	B3	B2	C24
1	259	I/O	–	–	–	–	B4	C22
1	260	I/O	–	–	–	–	A4	A24
1	261	I/O	–	–	–	–	A3	B24
1	262	I/O	–	–	–	–	B3	C23
1	263	I/O	–	–	–	–	A2	B25
–	264	GNDIO	GND	GND	GND	GND	GND	GND
–	265	–	–	–	–	–	–	–

Pin Name	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
MSEL0 (6)	18	25	29	F11	J17	P1
MSEL1 (6)	19	26	30	F10	J16	P2
nSTATUS (6)	57	82	92	M4	U9	AF15
nCONFIG (6)	22	29	33	G10	K17	R1
DCLK (6)	93	132	152	G2	J3	N25
CONF_DONE (6)	58	83	93	M3	U8	AE15
INIT_DONE (4)	121	178	206	D6	E11	A16
nCE (6)	91	130	150	H5	K2	P26
nCEO (6)	128	185	213	A9	C10	A12
nWS (2)	103	145	164	C2	K5	H22
nRS (2)	102	142	161	D2	J6	H24
nCS (2)	101	141	160	D3	H5	J24
CS (2)	98	138	157	E3	M2	K25
RDYnBSY (2)	120	177	205	E6	E10	B16
CLKUSR (2)	119	176	204	F6	F10	C16
DATA7 (2)	104	146	166	C1	H6	G23
DATA6 (2)	105	150	169	B2	G4	F24
DATA5 (2)	109	157	181	B3	B2	C24
DATA4 (2)	111	160	185	C3	C5	A25
DATA3 (2)	112	163	189	C4	B6	B22
DATA2 (2)	115	168	195	D5	E8	B20
DATA1 (2)	117	173	200	C5	F9	B18
DATA0 (6), (7)	94	133	153	G3	J2	M26
TDI (6)	90	129	149	H2	K3	P25
TDO (6)	123	180	208	A4	C9	B15
TCK (6)	52	76	87	M9	U10	AE12
TMS (6)	51	75	86	M10	U11	AF11
TRST (6)	129	186	214	A10	B10	B12
Dedicated Fast I/Os	127, 124, 53, 56	184, 181, 77, 81	212, 209, 88, 91	A8, A5, M8, M5	D10, B9, T10, T9	A13, A15, AF12, AE14
CLK1p	20	27	31	F9	K16	P3
CLK2p	92	131	151	G7	J4	N26
CLK3p	23	31	34	G8	H15	R4
CLK4p	95	134	154	F2	L2	M23
LOCK2 (10)	80	119	138	K3	N2	T24
LOCK4 (10)	78	116	135	L2	R3	V25
CLKLK_ENA(6), (11)	21	28	32	G9	K12	P4
CLKLK_OUT2p (9)	81	120	139	J2	M3	R23
CLKLK_FB2p	96	135	155	F4	N4	L25
DEV_CLRn (4)	97	137	156	E4	L5	L23
DEV_OE (4)	84	124	143	J3	L4	R26
VCCINT	1, 16, 36, 55, 73, 86, 108, 125	1, 23, 52, 79, 105,126, 156, 182	1, 27, 60, 90, 122, 145, 179, 210	A7, B1, B12, F1, F12, H1, H12, M7	G6, G11, F7, H9, H12, J8, K11, L7, L10, M8, M13, N5, N12	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1, M25, R2, T22, U4, Y26
VCCIO1	107	136	177	A2	E6, G8	C14, A26

Pin Name	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
VCCIO2	5	189, 208	229	A11	F12, H10	A1, C12
VCCIO3	144	8	12	D12	J11, G13	M5, C1
VCCIO4	45	80	67	K12	L12, N14	AD1, P5
VCCIO5	28	42, 53	45	M11	M11, P13	AD12, AF1
VCCIO6	89	115	148	M2	L9, N7, P6	AF26, AD14
VCCIO7	61	86	97, 120	K1	K8, M6	P22, AD26
VCCIO8	116	172	199	D1	F5, H7	C26, M22
VCC_CKLK2 (3)	85	125	144	G6	J7	P23
VCC_CKLK4 (3)	100	140	159	D4	K6	K24
VCC_CKOUT2 (8)	83	123	142	H4	P3	R25
GND	4, 12, 17, 34, 42, 54, 72, 74, 77, 87, 106, 126, 134	10, 16, 24, 39, 43, 64, 78, 95, 114, 118, 127, 143, 149, 169, 183, 199	19, 26, 28, 42, 56, 78, 89, 108, 132, 137, 146, 162, 165, 188, 211, 218, 240	A1, A6, A12, E1, E12, G1, G12, J1, J12, M1, M6, M12	D4, D15, E5, E14, F6, F13, G7, G9, G12, H8, H11, J9, J10, K9, K10, L8, L11, M7, M12, N6, N13, P5, P14, R4, R15	AB4,AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24
GND_CKLK2 (3)	88	128	147	G5	K7	P24
GND_CKLK4 (3)	99	139	158	E2	L6	L22
GND_CKOUT2 (8)	82	122	141	H3	P2	R24
No Connect (N.C.)	–	153, 154, 155	2, 3, 4, 54, 55, 57, 58,59,64, 80, 83, 94, 104, 106, 111, 116, 121, 172, 173, 174, 175, 176, 178, 180, 182, 190, 197, 203, 216, 226, 233, 237	–	A1, A18, B1, B17, B18, C1, C16, C17, C18, C2, C3, C4, D1, D16, D17, D18, D2, D3, E1, E16, E17, E18, E2, E4, F1,F15, F16, F18, F4, J1, M14, N15, P1, P15, P16, P17, R1, R17, R2, T1, T18, T2, U1, U17, U2, U3, V1, V17, V18, V2	AA26, AA25, AA3, AA2, AA1, AA24, AA23, AB26, AB2, AB1, AB24, AB23, AB22, AC26, AC25, AC2, AC1, D2, D1, E4, E3, E2, J25, K26, K23, AA22, AA4, AA5, D25, D26, E22, E24, E25, E26, F1, F2, F22, F23, F25, F3, F4, F5, G1, G2, G22, G24, G26, G3, G4, G5, H3, H4, H5, J22, J26, J4, J5, K22, T25, T26, V22, W22, W25, W3, W4, W5, Y1, Y2, Y22, Y23, Y24, Y25, Y3, Y4, Y5
Total User I/O Pins (12)	92	148	151	93	196	196

Notes:

(1) For the 144-pin, 208-pin, and 240-pin QFP packages, four unique VCCIO levels are supported. The VCCIO pins for I/O banks 1 and 8 must be at the same level. The VCCIO pins for banks 6 and 7 form a single I/O bank. The VCCIO pins for I/O banks 4 and 5 must be at the same level. The VCCIO pins for I/O banks 2 and 3 must be at the same level. However, unique VREF settings are supported for each of the eight I/O banks.

(2) This pin can be used as a user I/O pin after configuration.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(6) This pin is a dedicated pin; it is not available as a user I/O pin.

(7) This pin is tri-stated in user mode.

(8) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(9) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(10) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(11) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(12) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.