Table 1 shows all pins for the EP2A40 672-pin FineLine BGA, 724-pin ball-grid array (BGA), and 1,020-pin FineLine BGA

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
8	IO	TrueDiff_TX01p	A23	C25	D32	no
8	IO	TrueDiff_TX01n (2)	B23	C24	D31	no
8	IO	TrueDiff_TX02n (2)	A24	C27	E29	no
8	IO	TrueDiff_TX02p	B24	C26	E30	no
-	VCCIO		VCCIO8	VCCIO8	VCCIO8	
8	IO	TrueDiff_TX03p	C24	D25	E32	no
8	IO	TrueDiff_TX03n (2)	C23	D24	E31	no
8	IO	nWS (3)	F22	J20	J25	
8	IO	TrueDiff_TX04n (2)	C26	D27	F29	no
8	IO	TrueDiff_TX04p	C25	D26	F30	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
8	IO	TrueDiff_TX05p	D24	E25	F32	no
8	IO	TrueDiff_TX05n (2)	D23	E24	F31	no
8	IO	nRS (3)	G22	J21	J26	
8	IO	TrueDiff_TX06n (2)	D26	E27	G29	no
8	IO	TrueDiff_TX06p	D25	E26	G30	no
-	GNDIO		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
8	IO	TrueDiff_TX07p	E24	F25	G32	no
8	IO	TrueDiff_TX07n (2)	E23	F24	G31	no
8	IO	nCS (3)	G21	K20	K25	
8	IO	TrueDiff_TX08n (2)	E26	F27	H31	no
8	IO	TrueDiff_TX08p	E25	F26	H32	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
8	IO	TrueDiff_TX09p	F24	G25	J29	no
8	IO	TrueDiff_TX09n (2)	F23	G24	J30	no
8	IO	CS (3)	H22	K21	K24	
8	IO	TrueDiff_TX10n (2)	F26	G27	J31	no
8	IO	TrueDiff_TX10p	F25	G26	J32	no
-	VCCIO		VCCIO8	VCCIO8	VCCIO8	
8	IO	TrueDiff_TX11p	G24	H25	K30	no
8	IO	TrueDiff_TX11n (2)	G23	H24	K29	no
8	IO	DEV_CLRn (4)	H21	K19	K26	
8	IO	TrueDiff_TX12n (2)	G26	H27	K31	no
8	IO	TrueDiff_TX12p	G25	H26	K32	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
8	IO	TrueDiff_TX13p	H24	J25	L30	no
8	IO	TrueDiff_TX13n (2)	H23	J24	L29	no
8	IO		J20	G22	H27	
8	IO	TrueDiff_TX14n (2)	H26	J27	L31	no
8	IO	TrueDiff_TX14p	H25	J26	M31	no
-	GNDIO		GND	GND	GND	
8	IO	TrueDiff_TX15p	J23	K25	N31	no
8	IO	TrueDiff_TX15n (2)	J24	K24	M32	no
8	IO	TXLOCK1 (5)	J21	L18	L24	
8	IO	TrueDiff_TX16n (2)	J26	L25	N29	no
8	IO	TrueDiff_TX16p	J25	L24	N30	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
8	IO	TrueDiff_TX17p	K24	L27	P30	no

Table 1. EP2A40 Device Pin-Outs						
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**672-Pin FineLine BGA**	**724-Pin BGA**	**1020-Pin FineLine BGA**	**HSTL Class II Output Support (1)**
8	IO	TrueDiff_TX17n (2)	K23	L26	P29	no
8	IO	LOCK4 (5)	K20	L21	K23	
8	IO	TrueDiff_TX18n (2)	K26	M27	R29	no
8	IO	TrueDiff_TX18p	K25	M26	R30	no
-	VCCIO		VCCIO8	VCCIO8	VCCIO8	
8	IO	TXCLK_OUT1p (6)	L24	M25	P32	no
8	IO	TXCLK_OUT1n (2)	L23	M24	P31	no
8	IO	DATA6 (3)	L20	K22	M25	
8	IO		M26	N27	R32	no
8	IO		M25	N26	R31	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	VSS	
8	IO		-	-	M28	
8	IO		-	F23	F28	
8	IO		J19	G19	M24	
8	IO		-	-	H28	
8	IO		-	-	K27	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDIO		GND	GND	GND	
8	IO		-	-	H29	
8	IO		-	G23	G28	
8	IO		K19	J22	M27	
8	IO		-	-	J28	
8	IO		-	-	L27	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
8	IO		-	-	H30	
8	IO		-	H23	G27	
8	IO		L18	H21	L25	
8	IO		-	-	K28	
8	IO		-	-	L26	
-	VCCIO		VCCIO8	VCCIO8	VCCIO8	
8	IO		-	-	N28	
8	IO		-	H22	J27	
8	IO		L19	G20	M26	
8	IO		-	-	L28	
8	IO		-	-	N27	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
8	IO		-	-	M29	
8	IO		-	L22	L23	
8	IO		M18	H19	N26	
8	IO		-	J23	L22	
8	IO		-	-	H26	
-	GNDIO		GND	GND	GND	
8	IO		-	-	M30	
8	IO		-	H18	M23	
8	IO		M19	H16	M22	
8	IO		-	M23	N25	
8	IO		-	-	P27	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
8	IO		-	-	N24	
8	IO		-	L20	N23	
8	IO		N18	M21	P26	

Table 1. EP2A40 Device Pin-Outs						
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**672-Pin FineLine BGA**	**724-Pin BGA**	**1020-Pin FineLine BGA**	**HSTL Class II Output Support (1)**
8	IO		-	M22	N22	
8	IO		-	-	P25	
-	VCCIO		VCCIO8	VCCIO8	VCCIO8	
8	IO	DATA7 (3)	M20	L23	P28	
8	IO		-	M20	N21	
8	IO		-	N18	P22	
8	IO		-	-	P21	
8	IO		-	-	R27	
8	VREFC8 (7)		J22	L19	P23	
-	GND_CKLK6 (8)		K22	N21	R24	
-	VCC_CKLK6 (8)		K21	M19	P24	
-	VCC_CKLK4 (8)		L21	M18	R23	
-	GND_CKLK4 (8)		L22	N20	T24	
8	IO		-	-	R26	
8	IO		N19	N19	R25	
8	IO		-	P23	R22	
8	IO		-	-	R21	
-	GNDIO		GND	GND	GND	
8	IO	CLKLK_FB2n (2)	N26	N25	R28	
9	CLKLK_FB2p (9), (10)		N25	N24	T28	
8	IO	CLK4n (2)	M23	N22	T31	
8	CLK4p		M24	N23	T32	
8	IO	CLK2n (2)	N24	P25	T30	
-	VCCIO		VCCIO8	VCCIO8	VCCIO8	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
-	GNDIO		GND	GND	GND	
-	nIO_PULLUP (9), (11)		N20	P22	T26	
8	DATA0 (9)(12)		P20	P18	T25	
8	DCLK (9)		R20	P21	T27	
8	CLK2p		N23	P24	T29	
8	nCE (9)		U20	T23	T22	
8	TDI (9)		T20	T22	T21	
-	GNDIO		GND	GND	GND	
-	GND_CKLK2 (8)		T22	P20	T23	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	VCC_CKLK2 (8)		T21	P19	U23	
-	VCCIO		VCCIO7	VCCIO7	VCCIO7	
7	IO	DEV_OE (4)	V21	R21	U22	
-	VCC_CKOUT2 (13)		P21	U23	U24	
-	GND_CKOUT2 (13)		R21	R18	V23	
9	CLKLK_OUT2p (9), (14)		P25	P27	U26	
7	IO	CLKLK_OUT2n (2)	P26	P26	U27	
-	GNDIO		GND	GND	GND	
7	IO	CLK6n (2)	P23	R22	U31	
7	CLK6p		P24	R23	U32	
7	IO	LOCK2 (5)	W22	R19	U21	
7	IO	CLK8n (2)	R25	R24	U30	
7	CLK8p		R26	R25	U29	

Table 1. EP2A40 Device Pin-Outs						
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**672-Pin FineLine BGA**	**724-Pin BGA**	**1020-Pin FineLine BGA**	**HSTL Class II Output Support (1)**
-	VCC_CKLKA (15)		U22	U22	U25	
-	VCC_CKLK8 (8)		U21	T18	W24	
-	GND_CKLK8 (8)		V22	R20	V24	
-	VCCIO		VCCIO7	VCCIO7	VCCIO7	
7	VREFC7 (7)		Y22	T19	V22	
7	IO		-	-	V21	
7	IO		P19	T20	U28	
7	IO		-	-	V25	
7	IO		-	-	V26	
7	IO		-	-	V28	
-	GNDIO		GND	GND	GND	
7	IO		-	-	V27	
7	IO		P18	U18	W21	
7	IO		-	-	W22	
7	IO		-	-	W23	
7	IO		-	-	Y21	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO		-	-	W25	
7	IO		-	T21	Y22	
7	IO		R19	U19	W26	
7	IO		-	-	Y23	
7	IO		-	-	W27	
-	VCCIO		VCCIO7	VCCIO7	VCCIO7	
7	IO		-	-	Y24	
7	IO		R18	V19	Y25	
7	IO		T19	U20	AA22	
7	IO		-	-	AA23	
7	IO		-	-	W28	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO		-	-	AB22	
7	IO		T18	V20	AA24	
7	IO		U18	U21	Y26	
7	IO		-	-	AB23	
7	IO		-	-	AA30	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDIO		GND	GND	GND	
7	IO		-	-	AA25	
7	IO		U19	V21	Y28	
7	IO		V19	Y19	Y27	
7	IO		-	-	AB24	
7	IO		-	-	AA29	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO		-	-	AC23	
7	IO		W21	AA19	AB28	
7	IO		V20	W20	AA26	
7	IO		-	-	AA27	
7	IO		-	-	AE29	
-	VCCIO		VCCIO7	VCCIO7	VCCIO7	
7	IO		-	-	AB26	
7	IO		AB22	W23	AC28	
7	IO		Y21	W21	AC25	

Table 1. EP2A40 Device Pin-Outs						
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**672-Pin FineLine BGA**	**724-Pin BGA**	**1020-Pin FineLine BGA**	**HSTL Class II Output Support (1)**
7	IO		-	-	AC26	
7	IO		-	-	AA28	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO		R23	R26	V31	no
7	IO		R24	R27	V32	no
7	IO		-	V22	AD25	
7	IO	TXCLK_OUT2n (2)	T23	T24	W31	no
7	IO	TXCLK_OUT2p (6)	T24	T25	W32	no
-	GNDIO		GND	GND	GND	
7	IO	TrueDiff_TX36p	U25	T26	V30	no
7	IO	TrueDiff_TX36n (2)	U26	T27	V29	no
7	IO		-	AA20	AD26	
7	IO	TrueDiff_TX35n (2)	U23	U26	W29	no
7	IO	TrueDiff_TX35p	U24	U27	W30	no
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO	TrueDiff_TX34p	V25	U24	Y30	no
7	IO	TrueDiff_TX34n (2)	V26	U25	Y29	no
7	IO		-	Y21	AB27	
7	IO	TrueDiff_TX33n (2)	V23	V24	AA32	no
7	IO	TrueDiff_TX33p	V24	V25	Y31	no
-	VCCIO		VCCIO7	VCCIO7	VCCIO7	
7	IO	TrueDiff_TX32p	W25	W26	AA31	no
7	IO	TrueDiff_TX32n (2)	W26	W27	AB31	no
7	IO		-	Y23	AC27	
7	IO	TrueDiff_TX31n (2)	W23	W24	AB29	no
7	IO	TrueDiff_TX31p	W24	W25	AB30	no
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO	TrueDiff_TX30p	Y25	Y26	AC32	no
7	IO	TrueDiff_TX30n (2)	Y26	Y27	AC31	no
7	IO	TXLOCK2 (5)	AA22	W22	AB25	
7	IO	TrueDiff_TX29n (2)	Y23	Y24	AC29	no
7	IO	TrueDiff_TX29p	Y24	Y25	AC30	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDIO		GND	GND	GND	
7	IO	TrueDiff_TX28p	AA25	AA26	AD32	no
7	IO	TrueDiff_TX28n (2)	AA26	AA27	AD31	no
7	IO		-	Y22	AD28	
7	IO	TrueDiff_TX27n (2)	AA23	AA24	AD29	no
7	IO	TrueDiff_TX27p	AA24	AA25	AD30	no
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO	TrueDiff_TX26p	AB25	AB26	AE32	no
7	IO	TrueDiff_TX26n (2)	AB26	AB27	AE31	no
7	IO		-	AA23	AE28	
7	IO	TrueDiff_TX25n (2)	AB23	AB24	AF31	no
7	IO	TrueDiff_TX25p	AB24	AB25	AF32	no
-	VCCIO		VCCIO7	VCCIO7	VCCIO7	
7	IO	TrueDiff_TX24p	AC25	AC26	AF30	no
7	IO	TrueDiff_TX24n (2)	AC26	AC27	AF29	no
7	IO		-	AA22	AD27	
7	IO	TrueDiff_TX23n (2)	AC23	AC24	AG31	no
7	IO	TrueDiff_TX23p	AC24	AC25	AG32	no

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
7	IO	TrueDiff_TX22p	AD25	AD26	AG30	no
7	IO	TrueDiff_TX22n (2)	AD26	AD27	AG29	no
7	IO		-	AB23	AE27	
7	IO	TrueDiff_TX21n (2)	AD23	AD24	AH31	no
7	IO	TrueDiff_TX21p	AD24	AD25	AH32	no
-	GNDIO		GND	GND	GND	
7	IO	TrueDiff_TX20p	AF24	AE26	AH30	no
7	IO	TrueDiff_TX20n (2)	AE24	AE27	AH29	no
7	IO	TrueDiff_TX19n (2)	AF23	AE24	AJ31	no
7	IO	TrueDiff_TX19p	AE23	AE25	AJ32	no
-	VCCIO		VCCIO7	VCCIO7	VCCIO7	
6	IO	FlexDiff_TX01n (2)	AF22	AF25	AJ28	
6	IO	FlexDiff_TX01p	AE22	AG25	AK28	
6	IO	FlexDiff_TX57n (2)	-	-	AF26	
6	IO	FlexDiff_TX57p	-	-	AE26	
-	GNDIO		GND	GND	GND	
6	IO	FlexDiff_TX02n (2)	AD22	AG24	AL29	
6	IO	FlexDiff_TX02p	AC22	AF24	AM29	
6	IO	FlexDiff_TX58n (2)	-	-	AH27	
6	IO	FlexDiff_TX58p	-	-	AG27	
6	IO	FlexDiff_TX03n (2)	AF21	AD23	AL28	
6	IO	FlexDiff_TX03p	AE21	AE23	AM28	
6	IO	FlexDiff_TX59n (2)	-	-	AH26	
6	IO	FlexDiff_TX59p	-	-	AG26	
-	VCCIO		VCCIO6	VCCIO6	VCCIO6	
6	IO	FlexDiff_TX04n (2)	AD21	AG23	AJ27	
6	IO	FlexDiff_TX04p	AC21	AF23	AK27	
6	IO	FlexDiff_TX60n (2)	-	-	AH25	
6	IO	FlexDiff_TX60p	-	-	AG25	
6	IO	FlexDiff_TX05n (2)	AF20	AB22	AL27	
6	IO	FlexDiff_TX05p	AE20	AC22	AM27	
6	IO	FlexDiff_TX06n (2)	AD20	AE22	AJ26	
6	IO	FlexDiff_TX06p	AC20	AD22	AK26	
-	GNDIO		GND	GND	GND	
6	IO	FlexDiff_TX07n (2)	AB20	AF22	AL26	
6	IO	FlexDiff_TX07p	AA20	AG22	AM26	
6	IO	FlexDiff_TX08n (2)	AF19	AC21	AG24	
6	IO	FlexDiff_TX08p	AE19	AB21	AH24	
6	IO	FlexDiff_TX09n (2)	AD19	AD21	AJ25	
-	VCCIO		VCCIO6	VCCIO6	VCCIO6	
6	IO	FlexDiff_TX09p	AC19	AE21	AK25	
6	IO	FlexDiff_TX10n (2)	AB19	AG21	AL25	
6	IO	FlexDiff_TX10p	AA19	AF21	AM25	
6	IO	FlexDiff_TX61n (2)	-	-	AF24	
6	IO	FlexDiff_TX60p	-	-	AE24	
6	IO	FlexDiff_TX11n (2)	Y19	AB20	AJ24	
6	IO	FlexDiff_TX11p	W19	AC20	AK24	
6	IO	FlexDiff_TX62n (2)	-	-	AD24	
6	IO	FlexDiff_TX62p	-	-	AC24	
6	IO	FlexDiff_TX12n (2)	AF18	AE20	AL24	
-	GNDIO		GND	GND	GND	
6	IO	FlexDiff_TX12p	AE18	AD20	AM24	
6	IO	FlexDiff_TX63n (2)	-	-	AH23	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
6	IO	FlexDiff TX63p	-	-	AG23	
6	IO	FlexDiff TX13n (2)	AD18	AF20	AJ23	
6	IO	FlexDiff TX13p	AC18	AG20	AK23	
6	IO	FlexDiff TX64n (2)	-	-	AF23	
6	IO	FlexDiff TX64p	-	-	AE23	
6	IO	FlexDiff TX14n (2)	AB18	AC19	AG22	
6	IO	FlexDiff TX14p	AA18	AB19	AH22	
6	IO		AB21	AA18	AF22	
6	IO		AA21	Y18	AE22	
6	VREFC6 (7)		W20	Y17	AC18	
-	VCCIO		VCCIO6	VCCIO6	VCCIO6	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
-	GNDIO		GND	GND	GND	
6	IO	CDS ENA (16)	V18	Y16	AF17	
6	IO		Y20	AA17	AE21	
6	IO	FlexDiff TX15p	Y18	AD19	AK22	
6	IO	FlexDiff TX15n (2)	W18	AE19	AJ22	
6	IO	FlexDiff TX65p	-	-	AF20	
-	VCCIO		VCCIO6	VCCIO6	VCCIO6	
6	IO	FlexDiff TX65n (2)	-	-	AE20	
6	IO	FlexDiff TX16p	AF17	AG19	AM23	
6	IO	FlexDiff TX16n (2)	AE17	AF19	AL23	
6	IO	FlexDiff TX66p	-	-	AH21	
6	IO	FlexDiff TX66n (2)	-	-	AG21	
6	IO	FlexDiff TX17p	AD17	AC18	AL21	
-	GNDIO		GND	GND	GND	
6	IO	FlexDiff TX17n (2)	AC17	AB18	AL22	
6	IO	FlexDiff TX67p	-	-	AF19	
6	IO	FlexDiff TX67n (2)	-	-	AE19	
6	IO	FlexDiff TX18p	AB17	AE18	AK21	
6	IO	FlexDiff TX18n (2)	AA17	AD18	AJ21	
6	IO	FlexDiff TX68p	-	-	AH19	
6	IO	FlexDiff TX68n (2)	-	-	AG19	
6	IO	FlexDiff TX19p	Y17	AB17	AL20	
6	IO	FlexDiff TX19n (2)	W17	AC17	AM21	
6	IO	FlexDiff TX20p	AF16	AE17	AH20	
-	VCCIO		VCCIO6	VCCIO6	VCCIO6	
6	IO	FlexDiff TX20n (2)	AE16	AD17	AG20	
6	IO	FlexDiff TX21p	AD16	AF17	AK20	
6	IO	FlexDiff TX21n (2)	AC16	AG17	AJ20	
6	IO	FlexDiff TX22p	AB16	AB16	AK19	
6	IO	FlexDiff TX22n (2)	AA16	AC16	AJ19	
6	IO	FlexDiff TX23p	Y16	AD16	AM19	
6	IO	FlexDiff TX23n (2)	W16	AE16	AL19	
6	IO	FlexDiff TX24p	AF15	AG16	AH18	
6	IO	FlexDiff TX24n (2)	AE15	AF16	AG18	
-	GNDIO		GND	GND	GND	
6	IO	FlexDiff TX69p	-	-	AD20	
6	IO	FlexDiff TX69n (2)	-	-	AC20	
6	IO	FlexDiff TX25p	AD15	AB15	AK18	
6	IO	FlexDiff TX25n (2)	AC15	AC15	AJ18	
6	IO	FlexDiff TX70p	-	-	AD19	
6	IO	FlexDiff TX70n (2)	-	-	AC19	
-	VCCIO		VCCIO6	VCCIO6	VCCIO6	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
6	IO	FlexDiff TX26p	AB15	AE15	AM18	
6	IO	FlexDiff TX26n (2)	AA15	AD15	AL18	
6	IO	FlexDiff TX71p	-	-	AF18	
6	IO	FlexDiff TX71n (2)	-	-	AE18	
6	IO	FlexDiff TX27p	Y15	AF15	AK17	
-	GNDIO		GND	GND	GND	
6	IO	FlexDiff TX27n (2)	W15	AG15	AJ17	
6	IO	FlexDiff TX72p	-	-	AH17	
6	IO	FlexDiff TX72n (2)	-	-	AG17	
6	IO	FlexDiff TX28p	AD14	AG14	AM17	
6	IO	FlexDiff TX28n (2)	AC14	AF14	AL17	
-	VCCIO		VCCIO6	VCCIO6	VCCIO6	
-	VCCINT		VCCINT	VCCINT	VCCINT	
5	CONF_DONE (9)		AB14	AA15	AE17	
5	nSTATUS (9)		AA14	Y15	AD17	
5	FAST4 (17)		Y14	AA16	AC17	
-	GNDINT		GND	GND	GND	
-	GNDIO		GND	GND	GND	
5	FAST3 (17)		Y13	AC14	AC16	
5	TCK (9)		AA13	Y14	AD16	
5	TMS (9)		AB13	AB14	AE16	
-	VCCIO		VCCIO5	VCCIO5	VCCIO5	
5	IO	FlexDiff TX56n (2)	AC13	AD14	AL16	
5	IO	FlexDiff TX56p	AD13	AE14	AM16	
5	IO	FlexDiff TX73n (2)	-	-	AG16	
5	IO	FlexDiff TX73p	-	-	AH16	
5	IO	FlexDiff TX55n (2)	AE12	AF13	AJ16	
5	IO	FlexDiff TX55p	AF12	AG13	AK16	
5	IO	FlexDiff TX74n (2)	-	-	AC15	
5	IO	FlexDiff TX74p	-	-	AD15	
-	GNDIO		GND	GND	GND	
5	IO	FlexDiff TX54n (2)	AC12	AD13	AL15	
5	IO	FlexDiff TX54p	AD12	AE13	AM15	
5	IO	FlexDiff TX75n (2)	-	-	AC14	
5	IO	FlexDiff TX75p	-	-	AD14	
5	IO	FlexDiff TX53n (2)	AA12	AB13	AJ15	
5	IO	FlexDiff TX53p	AB12	AC13	AK15	
5	IO	FlexDiff TX76n (2)	-	-	AE15	
5	IO	FlexDiff TX76p	-	-	AF15	
-	VCCIO		VCCIO5	VCCIO5	VCCIO5	
5	IO	FlexDiff TX52n (2)	W12	AF12	AG15	
5	IO	FlexDiff TX52p	Y12	AG12	AH15	
5	IO	FlexDiff TX51n (2)	AE11	AD12	AL14	
5	IO	FlexDiff TX51p	AF11	AE12	AM14	
5	IO	FlexDiff TX50n (2)	AC11	AB12	AJ14	
5	IO	FlexDiff TX50p	AD11	AC12	AK14	
5	IO	FlexDiff TX49n (2)	AA11	AF11	AJ13	
5	IO	FlexDiff TX49p	AB11	AG11	AK13	
5	IO	FlexDiff TX48n (2)	W11	AD11	AG13	
-	GNDIO		GND	GND	GND	
5	IO	FlexDiff TX48p	Y11	AE11	AH13	
5	IO	FlexDiff TX47n (2)	AE10	AB11	AM12	
5	IO	FlexDiff TX47p	AF10	AC11	AL13	
5	IO	FlexDiff TX77n (2)	-	-	AG14	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
5	IO	FlexDiff TX77p	-	-	AH14	
5	IO	FlexDiff TX46n (2)	AC10	AD10	AJ12	
5	IO	FlexDiff TX46p	AD10	AE10	AK12	
5	IO	FlexDiff TX78n (2)	-	-	AE14	
5	IO	FlexDiff TX78p	-	-	AF14	
5	IO	FlexDiff TX45n (2)	AA10	AB10	AL11	
-	VCCIO		VCCIO5	VCCIO5	VCCIO5	
5	IO	FlexDiff TX45p	AB10	AC10	AL12	
5	IO	FlexDiff TX79n (2)	-	-	AE13	
5	IO	FlexDiff TX79p	-	-	AF13	
5	IO	FlexDiff TX44n (2)	W10	AF9	AL10	
5	IO	FlexDiff TX44p	Y10	AG9	AM10	
5	IO	FlexDiff TX80n (2)	-	-	AG12	
-	GNDIO		GND	GND	GND	
5	IO	FlexDiff TX80p	-	-	AH12	
5	IO	FlexDiff TX43n (2)	AE9	AD9	AJ11	
5	IO	FlexDiff TX43p	AF9	AE9	AK11	
5	IO		V9	AA11	AE12	
5	IO		AA6	AA13	AF16	
-	VCCIO		VCCIO5	VCCIO5	VCCIO5	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
5	VREFC5 (7)		V10	AA12	AD12	
-	VCCIO		VCCIO5	VCCIO5	VCCIO5	
5	IO		AB6	AA9	AE11	
5	IO		AB5	AA10	AF11	
5	IO	FlexDiff TX42p	AC9	AB9	AH11	
5	IO	FlexDiff TX42n (2)	AD9	AC9	AG11	
5	IO	FlexDiff TX81p	-	-	AG10	
5	IO	FlexDiff TX81n (2)	-	-	AH10	
5	IO	FlexDiff TX41p	AA9	AG8	AK10	
5	IO	FlexDiff TX41n (2)	AB9	AF8	AJ10	
5	IO	FlexDiff TX82p	-	-	AE10	
5	IO	FlexDiff TX82n (2)	-	-	AF10	
5	IO	FlexDiff TX40p	W9	AD8	AM9	
-	GNDIO		GND	GND	GND	
5	IO	FlexDiff TX40n (2)	Y9	AE8	AL9	
5	IO	FlexDiff TX83p	-	-	AC9	
5	IO	FlexDiff TX83n (2)	-	-	AD9	
5	IO	FlexDiff TX39p	AE8	AC8	AK9	
5	IO	FlexDiff TX39n (2)	AF8	AB8	AJ9	
5	IO	FlexDiff TX84p	-	-	AE9	
5	IO	FlexDiff TX84n (2)	-	-	AF9	
5	IO	FlexDiff TX38p	AC8	AF7	AM8	
5	IO	FlexDiff TX38n (2)	AD8	AG7	AL8	
5	IO	FlexDiff TX37p	AA8	AE7	AK8	
-	VCCIO		VCCIO5	VCCIO5	VCCIO5	
5	IO	FlexDiff TX37n (2)	AB8	AD7	AJ8	
5	IO	FlexDiff TX36p	W8	AB7	AH9	
5	IO	FlexDiff TX36n (2)	Y8	AC7	AG9	
5	IO	FlexDiff TX35p	AE7	AG6	AM7	
-	GNDIO		GND	GND	GND	
5	IO	FlexDiff TX35n (2)	AF7	AF6	AL7	
5	IO	FlexDiff TX34p	AC7	AD6	AK7	
5	IO	FlexDiff TX34n (2)	AD7	AE6	AJ7	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
5	IO	FlexDiff_TX33p	AA7	AC6	AM6	
5	IO	FlexDiff_TX33n (2)	AB7	AB6	AL6	
-	VCCIO		VCCIO5	VCCIO5	VCCIO5	
5	IO	FlexDiff_TX85p	-	-	AE8	
5	IO	FlexDiff_TX85n (2)	-	-	AF8	
5	IO	FlexDiff_TX32p	AE6	AF5	AK6	
5	IO	FlexDiff_TX32n (2)	AF6	AG5	AJ6	
5	IO	FlexDiff_TX86p	-	-	AG8	
5	IO	FlexDiff_TX86n (2)	-	-	AH8	
-	GNDIO		GND	GND	GND	
5	IO	FlexDiff_TX31p	AC6	AE5	AM5	
5	IO	FlexDiff_TX31n (2)	AD6	AD5	AL5	
5	IO	FlexDiff_TX87p	-	-	AG7	
5	IO	FlexDiff_TX87n (2)	-	-	AH7	
5	IO	FlexDiff_TX30p	AE5	AF4	AM4	
-	GNDIO		GND	GND	GND	
5	IO	FlexDiff_TX30n (2)	AF5	AG4	AL4	
5	IO	FlexDiff_TX88p	-	-	AG6	
5	IO	FlexDiff_TX88n (2)	-	-	AH6	
5	IO	FlexDiff_TX29p	AC5	AG3	AK5	
5	IO	FlexDiff_TX29n (2)	AD5	AF3	AJ5	
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
4	IO	TrueDiff_RX19p	AF4	AE3	AJ1	no
4	IO	TrueDiff_RX19n (2)	AE4	AE4	AJ2	no
4	IO	TrueDiff_RX20n (2)	AF3	AE1	AH4	no
4	IO	TrueDiff_RX20p	AE3	AE2	AH3	no
-	GNDIO		GND	GND	GND	
4	IO	TrueDiff_RX21p	AD3	AD3	AH1	no
4	IO	TrueDiff_RX21n (2)	AD4	AD4	AH2	no
4	IO		-	AB5	AE6	
4	IO	TrueDiff_RX22n (2)	AD1	AD1	AG4	no
4	IO	TrueDiff_RX22p	AD2	AD2	AG3	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO	TrueDiff_RX23p	AC3	AC3	AG1	no
4	IO	TrueDiff_RX23n (2)	AC4	AC4	AG2	no
4	IO		-	AA6	AG5	
4	IO	TrueDiff_RX24n (2)	AC1	AC1	AF4	no
4	IO	TrueDiff_RX24p	AC2	AC2	AF3	no
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
4	IO	TrueDiff_RX25p	AB3	AB3	AF1	no
4	IO	TrueDiff_RX25n (2)	AB4	AB4	AF2	no
4	IO		-	AA5	AF5	
4	IO	TrueDiff_RX26n (2)	AB1	AB1	AE2	no
4	IO	TrueDiff_RX26p	AB2	AB2	AE1	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO	TrueDiff_RX27p	AA3	AA3	AD3	no
4	IO	TrueDiff_RX27n (2)	AA4	AA4	AD4	no
4	IO		-	Y6	AE5	
4	IO	TrueDiff_RX28n (2)	AA1	AA1	AD2	no
4	IO	TrueDiff_RX28p	AA2	AA2	AD1	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDIO		GND	GND	GND	
4	IO	TrueDiff_RX29p	Y3	Y3	AC3	no

Table 1. EP2A40 Device Pin-Outs						
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**672-Pin FineLine BGA**	**724-Pin BGA**	**1020-Pin FineLine BGA**	**HSTL Class II Output Support (1)**
4	IO	TrueDiff_RX29n (2)	Y4	Y4	AC4	no
4	IO		-	Y5	AC6	
4	IO	TrueDiff_RX30n (2)	Y1	Y1	AC2	no
4	IO	TrueDiff_RX30p	Y2	Y2	AC1	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO	TrueDiff_RX31p	W3	W3	AB3	no
4	IO	TrueDiff_RX31n (2)	W4	W4	AB4	no
4	IO		-	W6	AD5	
4	IO	TrueDiff_RX32n (2)	W1	W1	AB2	no
4	IO	TrueDiff_RX32p	W2	W2	AA2	no
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
4	IO	TrueDiff_RX33p	V3	V3	Y2	no
4	IO	TrueDiff_RX33n (2)	V4	V4	AA1	no
4	IO		-	Y7	AE7	
4	IO	TrueDiff_RX34n (2)	V1	U3	Y4	no
4	IO	TrueDiff_RX34p	V2	U4	Y3	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO	TrueDiff_RX35p	U3	U1	W1	no
4	IO	TrueDiff_RX35n (2)	U4	U2	W2	no
4	IO		-	AA8	AB6	
4	IO	TrueDiff_RX36n (2)	U1	T1	W4	no
4	IO	TrueDiff_RX36p	U2	T2	W3	no
-	GNDIO		GND	GND	GND	
4	IO		-	W5	AA5	
4	IO		U8	T7	AD6	
4	IO		Y5	W7	AD7	
4	IO	RXCLK_IN2n (2)	R3	R1	V1	no
4	IO	RXCLK_IN2p	R4	R2	V2	no
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO		-	-	AE4	
4	IO		AA5	Y9	AC5	
4	IO		Y6	W8	AD8	
4	IO		-	-	AB5	
4	IO		-	-	AA6	
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
4	IO		-	-	AE3	
4	IO		W5	V7	AC7	
4	IO		Y7	Y10	AC8	
4	IO		-	-	Y5	
4	IO		-	-	AB7	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO		-	-	AA4	
4	IO		-	-	AB8	
4	IO		W7	U6	Y6	
4	IO		W6	U5	AA7	
4	IO		-	-	AC10	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDIO		GND	GND	GND	
4	IO		-	-	AA3	
4	IO		-	-	AB9	
4	IO		V8	Y11	AB10	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
4	IO		U9	V8	AA8	
4	IO		-	-	Y7	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO		-	-	W5	
4	IO		U10	U7	AA9	
4	IO		T8	Y12	AA10	
4	IO		-	-	AB11	
4	IO		-	-	W6	
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
4	IO		-	-	Y8	
4	IO		T9	V9	AA11	
4	IO		T10	Y13	W7	
4	IO		-	-	Y9	
4	IO		-	-	Y10	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
4	IO		-	-	V3	
4	IO		R8	U8	Y11	
4	IO		R10	U9	W8	
4	IO		-	-	Y12	
4	IO		-	-	W11	
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
-	GNDIO		GND	GND	GND	
4	IO		-	-	V5	
4	IO	RXLOCK2 (5)	U7	V6	V8	
4	IO		P9	U10	V6	
4	IO		-	-	V7	
4	IO		-	-	W12	
4	VREFC4 (7)		V7	T9	V12	
-	GND_CKLK7 (8)		U6	R8	W10	
-	GND_CKLK7 (8)		V5	T10	W9	
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
-	VCC_CKLK7 (8)		V6	R9	V10	
-	VCC_CKLKA (15)		U5	T6	V4	
4	IO		R9	R7	U11	
4	IO		-	R6	V11	
4	IO	LOCK1 (5)	T7	T5	U8	
4	IO		P8	R5	U12	
4	IO		-	T8	U7	
-	VCC_CKLK1 (8)		T6	R10	V9	
-	GND_CKLK1 (8)		R6	P8	U10	
-	GNDIO		GND	GND	GND	
4	IO	CLKLK_FB1n (2)	R1	T3	U6	
10	CLKLK_FB1p (9), (10)		R2	T4	U5	
4	IO	CLK3n (2)	P4	R4	U4	
4	CLK3p		P3	R3	U3	
4	IO	CLK1n (2)	P2	P4	U2	
-	VCCIO		VCCIO4	VCCIO4	VCCIO4	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	GNDINT		GND	GND	GND	
-	GNDIO		GND	GND	GND	
4	nCONFIG (9)		P7	P6	T7	

Table 1. EP2A40 Device Pin-Outs						
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**672-Pin FineLine BGA**	**724-Pin BGA**	**1020-Pin FineLine BGA**	**HSTL Class II Output Support (1)**
4	PLL_ENA (9)(18)		R7	P7	T11	
-	VCCSEL (9)(19)		P6	P5	T8	
4	CLK1p		P1	P3	U1	
4	MSEL1 (9)		M7	N5	R7	
4	MSEL0 (9)		N7	P9	T12	
-	GNDIO		GND	GND	GND	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	VCC_CKOUT1 (13)		M6	P10	T9	
-	GND_CKOUT1 (13)		N6	N6	U9	
10	CLKLK_OUT1p (9), (14)		N4	P2	T5	
3	IO	CLKLK_OUT1n (2)	N3	P1	T6	
-	VCC_CKLK3 (8)		K5	N7	T10	
-	VCCIO		VCCIO3	VCCIO3	VCCIO3	
-	GND_CKLK3 (8)		L6	N8	R10	
3	IO		N8	M9	R4	
3	IO	CLK5n (2)	N1	N3	T4	
3	CLK5p		N2	N4	T3	
3	IO	LOCK3 (5)	L7	L6	R6	
3	IO		N9	M8	R8	
-	GNDIO		GND	GND	GND	
-	GND_CKLK5 (8)		J6	M7	R9	
-	GND_CKLK5 (8)		J5	N9	P10	
-	VCC_CKLK5 (8)		K6	N10	P9	
3	VREFC3 (7)		J7	M10	R11	
3	IO	CLK7n (2)	M4	M4	T2	
3	CLK7p		M3	M3	T1	
3	IO		-	-	R12	
3	IO		-	L10	P12	
3	IO		M8	L9	R5	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO		-	-	P11	
3	IO		M9	M6	P8	
3	IO		L9	L8	N12	
3	IO		-	-	P7	
3	IO		-	-	R3	
-	VCCIO		VCCIO3	VCCIO3	VCCIO3	
3	IO		-	-	N11	
3	IO		-	M5	P6	
3	IO		L8	H12	N10	
3	IO		-	-	N9	
3	IO		-	-	P5	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO		-	-	N8	
3	IO		-	H10	M11	
3	IO		K9	K8	M10	
3	IO		-	-	N7	
3	IO		-	-	M3	
-	GNDIO		GND	GND	GND	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
3	IO		-	-	M9	
3	IO		-	J8	N6	
3	IO		K8	K7	L11	
3	IO		-	-	M8	
3	IO		-	-	N5	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO		-	-	L10	
3	IO		H6	L5	K10	
3	IO		H7	H9	M7	
3	IO		-	-	L8	
3	IO		-	-	M4	
-	VCCIO		VCCIO3	VCCIO3	VCCIO3	
3	IO		-	-	M6	
3	IO		G6	G8	L5	
3	IO		H5	J7	K8	
3	IO		-	-	L6	
3	IO		-	-	H3	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO		-	-	K7	
3	IO		F5	J5	K5	
3	IO		G5	K6	J8	
3	IO		-	-	J5	
3	IO		-	-	M5	
-	GNDIO		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO	RXCLK_IN1p	M2	N2	R2	no
3	IO	RXCLK_IN1n (2)	M1	N1	R1	no
3	IO		-	-	J7	
3	IO	RXLOCK1 (5)	K7	L7	L7	
3	IO		-	-	H4	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO	TrueDiff_RX18p	K2	M2	P3	no
3	IO	TrueDiff_RX18n (2)	K1	M1	P4	no
3	IO		-	H7	K6	
3	IO	TrueDiff_RX17n (2)	K4	L2	P2	no
3	IO	TrueDiff_RX17p	K3	L1	P1	no
-	VCCIO		VCCIO3	VCCIO3	VCCIO3	
3	IO	TrueDiff_RX16p	J2	L4	N3	no
3	IO	TrueDiff_RX16n (2)	J1	L3	N4	no
3	IO		J8	K9	L9	
3	IO	TrueDiff_RX15n (2)	J4	K4	M1	no
3	IO	TrueDiff_RX15p	J3	K3	N2	no
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO	TrueDiff_RX14p	H2	J2	M2	no
3	IO	TrueDiff_RX14n (2)	H1	J1	L2	no
3	IO		-	J6	H5	
3	IO	TrueDiff_RX13n (2)	H4	J4	L4	no
3	IO	TrueDiff_RX13p	H3	J3	L3	no
-	GNDIO		GND	GND	GND	
3	IO	TrueDiff_RX12p	G2	H2	K1	no
3	IO	TrueDiff_RX12n (2)	G1	H1	K2	no

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
3	IO		-	H6	J6	
3	IO	TrueDiff_RX11n (2)	G4	H4	K4	no
3	IO	TrueDiff_RX11p	G3	H3	K3	no
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO	TrueDiff_RX10p	F2	G2	J1	no
3	IO	TrueDiff_RX10n (2)	F1	G1	J2	no
3	IO		-	H5	G5	
3	IO	TrueDiff_RX09n (2)	F4	G4	J4	no
3	IO	TrueDiff_RX09p	F3	G3	J3	no
-	VCCIO		VCCIO3	VCCIO3	VCCIO3	
3	IO	TrueDiff_RX08p	E2	F2	H1	no
3	IO	TrueDiff_RX08n (2)	E1	F1	H2	no
3	IO		-	G5	H6	
3	IO	TrueDiff_RX07n (2)	E4	F4	G2	no
3	IO	TrueDiff_RX07p	E3	F3	G1	no
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO	TrueDiff_RX06p	D2	E2	G3	no
3	IO	TrueDiff_RX06n (2)	D1	E1	G4	no
3	IO		-	G6	F5	
3	IO	TrueDiff_RX05n (2)	D4	E4	F2	no
3	IO	TrueDiff_RX05p	D3	E3	F1	no
-	GNDIO		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
3	IO	TrueDiff_RX04p	C2	D2	F3	no
3	IO	TrueDiff_RX04n (2)	C1	D1	F4	no
3	IO		-	F5	G6	
3	IO	TrueDiff_RX03n (2)	C4	D4	E2	no
3	IO	TrueDiff_RX03p	C3	D3	E1	no
-	VCCIO		VCCIO3	VCCIO3	VCCIO3	
3	IO	TrueDiff_RX02p	A3	C2	E3	no
3	IO	TrueDiff_RX02n (2)	B3	C1	E4	no
3	IO	TrueDiff_RX01n (2)	A4	C4	D2	no
3	IO	TrueDiff_RX01p	B4	C3	D1	no
-	VCCIO		VCCIO2	VCCIO2	VCCIO2	
2	IO	FlexDiff_RX29n (2)	C5	A3	D5	
2	IO	FlexDiff_RX29p	D5	B3	C5	
2	IO	FlexDiff_RX57n (2)	-	-	G7	
2	IO	FlexDiff_RX57p	-	-	H7	
2	IO	FlexDiff_RX30n (2)	A5	A4	B4	
2	IO	FlexDiff_RX30p	B5	B4	A4	
2	IO	FlexDiff_RX58n (2)	-	-	E6	
2	IO	FlexDiff_RX58p	-	-	F6	
-	GNDIO		GND	GND	GND	
2	IO	FlexDiff_RX31n (2)	C6	C5	B5	
2	IO	FlexDiff_RX31p	D6	D5	A5	
2	IO	FlexDiff_RX59n (2)	-	-	E7	
2	IO	FlexDiff_RX59p	-	-	F7	
2	IO	FlexDiff_RX32n (2)	A6	A5	D6	
2	IO	FlexDiff_RX32p	B6	B5	C6	
2	IO	FlexDiff_RX60n (2)	-	-	E8	
2	IO	FlexDiff_RX60p	-	-	F8	
-	VCCIO		VCCIO2	VCCIO2	VCCIO2	
2	IO	FlexDiff_RX33n (2)	E7	E6	B6	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
2	IO	FlexDiff_RX33p	F7	F6	A6	
2	IO	FlexDiff_RX34n (2)	C7	C6	D7	
2	IO	FlexDiff_RX34p	D7	D6	C7	
2	IO	FlexDiff_RX35n (2)	A7	A6	B7	
2	IO	FlexDiff_RX35p	B7	B6	A7	
2	IO	FlexDiff_RX36n (2)	G8	E7	F9	
2	IO	FlexDiff_RX36p	H8	F7	E9	
2	IO	FlexDiff_RX37n (2)	E8	C7	D8	
-	GNDIO		GND	GND	GND	
2	IO	FlexDiff_RX37p	F8	D7	C8	
2	IO	FlexDiff_RX38n (2)	C8	A7	B8	
2	IO	FlexDiff_RX38p	D8	B7	A8	
2	IO	FlexDiff_RX61n (2)	-	-	G9	
2	IO	FlexDiff_RX61p	-	-	H9	
2	IO	FlexDiff_RX39n (2)	A8	E8	D9	
2	IO	FlexDiff_RX39p	B8	F8	C9	
2	IO	FlexDiff_RX62n (2)	-	-	J9	
2	IO	FlexDiff_RX62p	-	-	K9	
2	IO	FlexDiff_RX40n (2)	G9	C8	B9	
-	VCCIO		VCCIO2	VCCIO2	VCCIO2	
2	IO	FlexDiff_RX40p	H9	D8	A9	
2	IO	FlexDiff_RX63n (2)	-	-	H10	
2	IO	FlexDiff_RX63p	-	-	J10	
2	IO	FlexDiff_RX41n (2)	E9	A8	D10	
2	IO	FlexDiff_RX41p	F9	B8	C10	
2	IO	FlexDiff_RX64n (2)	-	-	E10	
2	IO	FlexDiff_RX64p	-	-	F10	
2	IO	FlexDiff_RX42n (2)	C9	E9	F11	
2	IO	FlexDiff_RX42p	D9	F9	E11	
2	IO		E5	G10	G11	
2	IO		E6	G9	H11	
2	VREFC2 (7)		J9	H11	J12	
-	GNDIO		GND	GND	GND	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	VCCIO		VCCIO2	VCCIO2	VCCIO2	
2	IO		G7	G12	G16	
2	IO		F6	G11	H13	
2	IO	FlexDiff_RX43p	A9	C9	C11	
2	IO	FlexDiff_RX43n (2)	B9	D9	D11	
2	IO	FlexDiff_RX65p	-	-	E12	
-	GNDIO		GND	GND	GND	
2	IO	FlexDiff_RX65n (2)	-	-	F12	
2	IO	FlexDiff_RX44p	G10	A9	A10	
2	IO	FlexDiff_RX44n (2)	H10	B9	B10	
2	IO	FlexDiff_RX66p	-	-	J13	
2	IO	FlexDiff_RX66n (2)	-	-	K13	
2	IO	FlexDiff_RX45p	E10	E10	B12	
-	VCCIO		VCCIO2	VCCIO2	VCCIO2	
2	IO	FlexDiff_RX45n (2)	F10	F10	B11	
2	IO	FlexDiff_RX67p	-	-	E14	
2	IO	FlexDiff_RX67n (2)	-	-	F14	
2	IO	FlexDiff_RX46p	C10	C10	C12	
2	IO	FlexDiff_RX46n (2)	D10	D10	D12	
2	IO	FlexDiff_RX68p	-	-	G14	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
2	IO	FlexDiff_RX68n (2)	-	-	H14	
2	IO	FlexDiff_RX47p	A10	E11	B13	
2	IO	FlexDiff_RX47n (2)	B10	F11	A12	
2	IO	FlexDiff_RX48p	G11	C11	E13	
-	GNDIO		GND	GND	GND	
2	IO	FlexDiff_RX48n (2)	H11	D11	F13	
2	IO	FlexDiff_RX49p	E11	A11	C13	
2	IO	FlexDiff_RX49n (2)	F11	B11	D13	
2	IO	FlexDiff_RX50p	C11	E12	C14	
2	IO	FlexDiff_RX50n (2)	D11	F12	D14	
2	IO	FlexDiff_RX51p	A11	C12	A14	
2	IO	FlexDiff_RX51n (2)	B11	D12	B14	
2	IO	FlexDiff_RX52p	G12	A12	E15	
2	IO	FlexDiff_RX52n (2)	H12	B12	F15	
-	VCCIO		VCCIO2	VCCIO2	VCCIO2	
2	IO	FlexDiff_RX69p	-	-	G15	
2	IO	FlexDiff_RX69n (2)	-	-	H15	
2	IO	FlexDiff_RX53p	E12	E13	C15	
2	IO	FlexDiff_RX53n (2)	F12	F13	D15	
2	IO	FlexDiff_RX70p	-	-	J14	
2	IO	FlexDiff_RX70n (2)	-	-	K14	
2	IO	FlexDiff_RX54p	C12	C13	A15	
2	IO	FlexDiff_RX54n (2)	D12	D13	B15	
-	GNDIO		GND	GND	GND	
2	IO	FlexDiff_RX71p	-	-	J15	
2	IO	FlexDiff_RX71n (2)	-	-	K15	
2	IO	FlexDiff_RX55p	A12	A13	C16	
2	IO	FlexDiff_RX55n (2)	B12	B13	D16	
2	IO	FlexDiff_RX72p	-	-	E16	
2	IO	FlexDiff_RX72n (2)	-	-	F16	
2	IO	FlexDiff_RX56p	C13	C14	A16	
2	IO	FlexDiff_RX56n (2)	D13	D14	B16	
-	VCCIO		VCCIO2	VCCIO2	VCCIO2	
-	GNDINT		GND	GND	GND	
1	TRST (9)		E13	H13	K16	
1	nCEO (9)		F13	G13	J16	
1	FAST1 (17)		G13	E14	H16	
-	VCCINT		VCCINT	VCCINT	VCCINT	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
1	FAST2 (17)		G14	H14	J17	
1	TDO (9)		F14	F14	H17	
-	GNDINT		GND	GND	GND	
-	GNDIO		GND	GND	GND	
1	IO	FlexDiff_RX28n (2)	D14	B14	B17	
1	IO	FlexDiff_RX28p	C14	A14	A17	
1	IO	FlexDiff_RX73n (2)	-	-	F17	
1	IO	FlexDiff_RX73p	-	-	E17	
1	IO	INIT_DONE/FlexDiff_RX27n (2), (3)	H15	B15	D17	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
1	IO	FlexDiff_RX27p	G15	A15	C17	
1	IO	FlexDiff_RX74n (2)	-	-	K19	
1	IO	FlexDiff_RX74p	-	-	K20	
1	IO	FlexDiff_RX26n (2)	F15	D15	B18	

Table 1. EP2A40 Device Pin-Outs						
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**672-Pin FineLine BGA**	**724-Pin BGA**	**1020-Pin FineLine BGA**	**HSTL Class II Output Support (1)**
1	IO	RDYnBSY/FlexDiff_RX26p (3)	E15	C15	A18	
-	GNDIO		GND	GND	GND	
1	IO	FlexDiff_RX75n (2)	-	-	J18	
1	IO	FlexDiff_RX75p	-	-	J19	
1	IO	FlexDiff_RX25n (2)	D15	F15	D18	
1	IO	FlexDiff_RX25p	C15	E15	C18	
1	IO	FlexDiff_RX76n (2)	-	-	H18	
1	IO	FlexDiff_RX76p	-	-	G18	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
1	IO	CLKUSR/FlexDiff_RX24n (2), C984(3)	B15	B16	F18	
1	IO	FlexDiff_RX24p	A15	A16	E18	
1	IO	FlexDiff_RX23n (2)	H16	D16	B19	
1	IO	FlexDiff_RX23p	G16	C16	A19	
1	IO	FlexDiff_RX22n (2)	F16	F16	D19	
1	IO	DATA1 / FlexDiff_RX22p (3)	E16	E16	C19	
1	IO	FlexDiff_RX21n (2)	D16	B17	D20	
1	IO	FlexDiff_RX21p	C16	A17	C20	
1	IO	FlexDiff_RX20n (2)	B16	D17	F20	
-	GNDIO		GND	GND	GND	
1	IO	FlexDiff_RX20p	A16	C17	E20	
1	IO	FlexDiff_RX19n (2)	H17	F17	A21	
1	IO	FlexDiff_RX19p	G17	E17	B20	
1	IO	FlexDiff_RX77n (2)	-	-	F19	
1	IO	FlexDiff_RX77p	-	-	E19	
1	IO	FlexDiff_RX18n (2)	F17	D18	D21	
1	IO	FlexDiff_RX18p	E17	C18	C21	
1	IO	FlexDiff_RX78n (2)	-	-	H19	
1	IO	FlexDiff_RX78p	-	-	G19	
1	IO	FlexDiff_RX17n (2)	D17	F18	B22	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
1	IO	FlexDiff_RX17p	C17	E18	B21	
1	IO	FlexDiff_RX79n (2)	-	-	J20	
1	IO	FlexDiff_RX79p	-	-	H20	
1	IO	FlexDiff_RX16n (2)	B17	B19	B23	
1	IO	FlexDiff_RX16p	A17	A19	A23	
1	IO	FlexDiff_RX80n (2)	-	-	F21	
1	IO	FlexDiff_RX80p	-	-	E21	
1	IO	FlexDiff_RX15n (2)	H18	D19	D22	
1	IO	FlexDiff_RX15p	G18	C19	C22	
1	IO		G20	G16	G20	
1	IO	DATA2 (3)	H20	H15	G17	
-	GNDIO		GND	GND	GND	
-	GNDINT		GND	GND	GND	
-	VCCINT		VCCINT	VCCINT	VCCINT	
1	VREFC1 (7)		E22	H17	K18	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
1	IO		F21	G18	H21	
1	IO		E21	G17	G21	
1	IO	DATA3/FlexDiff_RX14p (3)	F18	F19	E22	
1	IO	FlexDiff_RX14n (2)	E18	E19	F22	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
1	IO	FlexDiff_RX81p	-	-	H22	
1	IO	FlexDiff_RX81n (2)	-	-	G22	
1	IO	FlexDiff_RX13p	D18	B20	C23	
1	IO	FlexDiff_RX13n (2)	C18	A20	D23	
1	IO	FlexDiff_RX82p	-	-	H23	
1	IO	FlexDiff_RX82n (2)	-	-	G23	
1	IO	FlexDiff_RX12p	B18	D20	A24	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
1	IO	FlexDiff_RX12n (2)	A18	C20	B24	
1	IO	FlexDiff_RX83p	-	-	F23	
1	IO	FlexDiff_RX83n (2)	-	-	E23	
1	IO	FlexDiff_RX11p	H19	F20	C24	
1	IO	FlexDiff_RX11n (2)	G19	E20	D24	
1	IO	FlexDiff_RX84p	-	-	H24	
1	IO	FlexDiff_RX84n (2)	-	-	G24	
1	IO	FlexDiff_RX10p	F19	B21	A25	
1	IO	FlexDiff_RX10n (2)	E19	A21	B25	
1	IO	FlexDiff_RX09p	D19	D21	C25	
-	GNDIO		GND	GND	GND	
1	IO	FlexDiff_RX09n (2)	C19	C21	D25	
1	IO	FlexDiff_RX08p	B19	F21	E24	
1	IO	FlexDiff_RX08n (2)	A19	E21	F24	
1	IO	FlexDiff_RX07p	F20	B22	A26	
1	IO	FlexDiff_RX07n (2)	E20	A22	B26	
1	IO	FlexDiff_RX06p	D20	D22	C26	
1	IO	FlexDiff_RX06n (2)	C20	C22	D26	
1	IO	FlexDiff_RX05p	B20	F22	A27	
1	IO	FlexDiff_RX05n (2)	A20	E22	B27	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
1	IO	FlexDiff_RX85p	-	-	H25	
1	IO	FlexDiff_RX85n (2)	-	-	G25	
1	IO	FlexDiff_RX04p	D21	B23	C27	
1	IO	FlexDiff_RX04n (2)	C21	A23	D27	
1	IO	FlexDiff_RX86p	-	-	F25	
1	IO	FlexDiff_RX86n (2)	-	-	E25	
1	IO	FlexDiff_RX03p	B21	D23	A28	
1	IO	DATA5/FlexDiff_RX03n (2), (3)	A21	C23	B28	
-	GNDIO		GND	GND	GND	
1	IO	FlexDiff_RX87p	-	-	F26	
1	IO	FlexDiff_RX87n (2)	-	-	E26	
1	IO	FlexDiff_RX02p	D22	B24	A29	
1	IO	FlexDiff_RX02n (2)	C22	A24	B29	
1	IO	FlexDiff_RX88p	-	-	F27	
1	IO	FlexDiff_RX88n (2)	-	-	E27	
1	IO	FlexDiff_RX01p	B22	B25	C28	
1	IO	DATA4 / FlexDiff_RX01n (2), (3)	A22	A25	D28	
-	VCCIO		VCCIO1	VCCIO1	VCCIO1	
	VCCINT		J10	L11	R15	
	VCCINT		J11	L13	R16	
	VCCINT		J12	L15	R17	
	VCCINT		J13	L17	R18	
	VCCINT		J14	V18	T14	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
	VCCINT		J15	J18	T16	
	VCCINT		J16	J12	T17	
	VCCINT		J17	W16	T19	
	VCCINT		J18	K11	U14	
	VCCINT		K10	M12	U16	
	VCCINT		K17	M14	U17	
	VCCINT		K18	M16	U19	
	VCCINT		L5	K17	V15	
	VCCINT		L10	K13	V16	
	VCCINT		L17	N13	V17	
	VCCINT		M5	N15	V18	
	VCCINT		M10	V13	P15	
	VCCINT		M17	W10	P16	
	VCCINT		M22	J10	P17	
	VCCINT		N10	P12	P18	
	VCCINT		N17	P16	W15	
	VCCINT		P10	W18	W16	
	VCCINT		P17	K15	W17	
	VCCINT		R5	R13	W18	
	VCCINT		R11	R15	N15	
	VCCINT		R17	V15	M16	
	VCCINT		R22	V11	M17	
	VCCINT		T5	T12	N18	
	VCCINT		T11	T14	Y15	
	VCCINT		T17	T16	AA16	
	VCCINT		U11	V17	AA17	
	VCCINT		U17	U17	Y18	
	VCCINT		V11	U11	AA15	
	VCCINT		V12	U13	AA18	
	VCCINT		V13	U15	M15	
	VCCINT		V14		M18	
	VCCINT		V15		M14	
	VCCINT		V16		N14	
	VCCINT		V17		P14	
	VCCINT				R14	
	VCCINT				V14	
	VCCINT				W14	
	VCCINT				Y14	
	VCCINT				AA14	
	VCCINT				M19	
	VCCINT				N19	
	VCCINT				P19	
	VCCINT				W19	
	VCCINT				Y19	
	VCCINT				AA19	
	VCCIO8		B26	B27	C32	
	VCCIO8		L26	K26	L32	
	VCCIO8		M21	N17	D30	
	VCCIO8			K18	T20	
	VCCIO8				M21	
	VCCIO7		N21	AF27	U20	
	VCCIO7		T26	R17	AA21	
	VCCIO7		AE26	V26	AB32	
	VCCIO7			W19	AK32	
	VCCIO7				AJ30	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
	VCCIO6		W14	AF18	AB17	
	VCCIO6		AF14	AG26	AC21	
	VCCIO6		AF25	W15	AM22	
	VCCIO6			Y20	AM30	
	VCCIO6				AK29	
	VCCIO5		W13	AF10	AB16	
	VCCIO5		AF2	AG2	AC12	
	VCCIO5		AF13	W13	AM11	
	VCCIO5			Y8	AM3	
	VCCIO5				AK4	
	VCCIO4		T1	AF1	AK1	
	VCCIO4		T2	R11	AJ3	
	VCCIO4		AE1	V2	AB1	
	VCCIO4			V10	U13	
	VCCIO4				AA12	
	VCCIO3		B1	B1	T13	
	VCCIO3		L1	K2	M12	
	VCCIO3		L2	N11	L1	
	VCCIO3			K10	C1	
	VCCIO3				D3	
	VCCIO2		A2	A2	L16	
	VCCIO2		A13	B10	K12	
	VCCIO2		H13	J13	A11	
	VCCIO2			H8	A3	
	VCCIO2				C4	
	VCCIO1		A14	A26	L17	
	VCCIO1		A25	B18	K21	
	VCCIO1		H14	J15	A22	
	VCCIO1			H20	A30	
	VCCIO1				C29	
	GND		B2	J14	AB15	
	GND		B13	J16	Y16	
	GND		B14	K12	Y17	
	GND		B25	L12	AB18	
	GND		E14	G15	K17	
	GND		K11	L14	L15	
	GND		K12	L16	N16	
	GND		K13	K16	N17	
	GND		K14	W12	L18	
	GND		K15	M11	AB19	
	GND		K16	M13	AB20	
	GND		L3	M15	AB13	
	GND		L4	M17	AB14	
	GND		L11	W14	L13	
	GND		L12	J11	L14	
	GND		L13	N12	L19	
	GND		L14	N16	L20	
	GND		L15	J17	M13	
	GND		L16	K14	N13	
	GND		L25	P11	P13	
	GND		M11	P17	R13	
	GND		M12	V14	T15	
	GND		M13	W11	U15	
	GND		M14	R12	V13	
	GND		M15	R16	W13	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
	GND		M16	W17	Y13	
	GND		N5	J9	AA13	
	GND		N11	T11	M20	
	GND		N12	T13	N20	
	GND		N13	T15	P20	
	GND		N14	T17	R19	
	GND		N15	V16	T18	
	GND		N16	V12	U18	
	GND		N22	U12	V19	
	GND		P5	U14	W20	
	GND		P11	U16	Y20	
	GND		P12	A1	AA20	
	GND		P13	A10	AB12	
	GND		P14	A18	L12	
	GND		P15	A27	L21	
	GND		P16	B2	AB21	
	GND		P22	B26	AC22	
	GND		R12	E5	AC11	
	GND		R13	E23	K11	
	GND		R14	G14	K22	
	GND		R15	K1	AD23	
	GND		R16	K5	AD10	
	GND		T3	K23	J24	
	GND		T4	K27	J23	
	GND		T12	V1	R20	
	GND		T13	V5	V20	
	GND		T14	V23	B1	
	GND		T15	V27	A2	
	GND		T16	AA14	A31	
	GND		T25	AC5	B32	
	GND		U12	AC23	AL32	
	GND		U13	AF2	AM31	
	GND		U14	AF26	AM2	
	GND		U15	AG1	AL1	
	GND		U16	AG10	AL3	
	GND		AE2	AG18	AK2	
	GND		AE13	AG27	AL2	
	GND		AE14	AA7	AK3	
	GND		AE25	AA21	AJ4	
	GND			G7	AH5	
	GND			G21	AL30	
	GND			W9	AK31	
	GND			J19	AL31	
	GND				AK30	
	GND				AJ29	
	GND				AH28	
	GND				B30	
	GND				C31	
	GND				B31	
	GND				C30	
	GND				D29	
	GND				E28	
	GND				C2	
	GND				B3	
	GND				B2	

Table 1. EP2A40 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	672-Pin FineLine BGA	724-Pin BGA	1020-Pin FineLine BGA	HSTL Class II Output Support (1)
	GND				C3	
	GND				D4	
	GND				E5	
	GND				AM13	
	GND				AM20	
	GND				A20	
	GND				A13	
	GND				N1	
	GND				Y1	
	GND				Y32	
	GND				N32	
	NC				AC13	
	NC				AF7	
	NC				G12	
	NC				AD11	
	NC				AF12	
	NC				G13	
	NC				AD13	
	NC				AF21	
	NC				G26	
	NC				AD18	
	NC				AF25	
	NC				H8	
	NC				AD21	
	NC				AF27	
	NC				H12	
	NC				AD22	
	NC				AF28	
	NC				J11	
	NC				AE25	
	NC				AG28	
	NC				J21	
	NC				AE30	
	NC				G8	
	NC				J22	
	NC				AF6	
	NC				G10	
Total User I/O Pins (20)			492	536	760	

Notes:

(1) The pins marked "no" in this column do not support the HSTL Class II output standard. All the unmarked pins support HSTL class II output in addition to other I/O standards.

(2) This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the differential channel. Pins with "p" suffix carry the positive signal for the differential channel.

(3) This pin can be used as a user I/O pin after configuration.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remians high if a periodic clock remains clocking. The LOCK function is optional, if the LOCK output is not used, this pin is a user I/O pin.

(6) Dedicated external clock output from one of the two LVDS TX PLLs. TXCLK_OUT1p is from TXPLL1, TXCLK_OUT2p is from TXPLL2.

(7) This pin is the dedicated power pin of VREF Control circuits (In addition to the programmable VREF pins) for each of the I/O banks. This pin can be connected to 2.5 V or 3.3 V if a voltage referenced I/O standard is used. Otherwise, it can be connected to 1.8 V, 2.5 V, or 3.3 V.

(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To insure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as VCCINT and should be connected to a 1.5-V power supply. If the ClockLock and ClockBoost circuitry is not used, this power or ground pin should be connected to the VCCINT or GND, respectively.

(9) This pin is a dedicted pin; it is not available as a user I/O pin.

(10) Dedicated external clock feedback from the general-purpose PLLs. CLKLK_FB1p feeds PLL1, CLKLK_FB2p feeds PLL2. The external clock feedback must use the same I/O standard as the external clock output and the global clock input to the general-purpose PLL. If this pin feature is not used, it should be connected to GND on the board.

(11) Dedicated input that is used to control whether weak active pull-up resistors are on for all I/O pins during power-up and configuration. A "0" means active pull-up resistors are enabled, a "1" (1.5 V, 1.8 V, 2.5 V, 3.3 V) means they are disabled.

(12) This pin is tri-stated in user mode.

(13) This pin is power or ground (Bank #9 and #10 in the Quartus II software) for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock output. To insure noise resistance, the power and ground supply to the PLL external output should be isolated from power and ground to the rest of the device. If the PLL or external output is not used, this power and ground pin should be connected to VCCIO or GND respectively.

(14) Dedicated external clock output from the general-purpose PLLs. CLKLK_OUT1p is from PLL1, CLKLK_OUT2p is from PLL2. Each dedicated clock output has its own VCCIO power for output standard selection. If this pin feature is not used, it should be connected to GND on the board.

(15) This pin is a dedicated power pin for the ClockLock and ClockBoost circuitry. It should be connected to the highest voltage level on the device. If possible, do not connect this pin to a noisy VCCIO pin.

(16) This is a dual-purpose pin for enabling the clock data synchronization (CDS) circuitry.

(17) This pin is a dedicated pin for driving the global fast lines within the entire device.

(18) This pin is a dedicated input pin that is the active high enable pin for all of the PLL circuits in the device. When de-asserted (low), all PLLs are reset to their default unlocked state and will stop clocking. Once re-asserted (can be 1.5 V, 1.8 V, 2.5 V, 3.3 V but should be the same as the VCCIO for that bank), the PLLs will lock again and start clocking. This PLL enable control can be selected on a per PLL basis. If this pin feature is not used, it should be connected to GND on the board.

Table 2 provides descriptions for all power, HSDI, and general-purpose PLL related pins.

Table 2. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
TrueDiff_RX[1..36]	Dual-purpose HSDI reciever channels 1 through 36. If not used, these pins are regular I/O pins.
TrueDiff_TX[1..36]	Dual-purpose HSDI transmitter channels 1 through 36. If not used, these pins are regular I/O pins.
FlexDiff_RX[1..88]	Dual-purpose Flexible-LVDS reciever channels 1 through 56. If not used, these pins are regular I/O pins.
FlexDiff_TX[1..88]	Dual-purpose Flexible-LVDS transmitter channels 1 through 56. If not used, these pins are regular I/O pins.
RXLOCK1	Dual-purpose pin for lock output of RX PLL1. If the PLL is not used, then this is a regular I/O pin.
RXLOCK2	Dual-purpose pin for lock output of RX PLL2. If the PLL is not used, then this is a regular I/O pin.
TXLOCK1	Dual-purpose pin for lock output of TX PLL1. If the PLL is not used, then this is a regular I/O pin.
TXLOCK2	Dual-purpose pin for lock output of TX PLL2. If the PLL is not used, then this is a regular I/O pin.
RXCLK_IN1	Dual-purpose clock input pin for RX PLL1.
RXCLK_IN2	Dual-purpose clock input pin for RX PLL2.
TXCLK_OUT1	Dual-purpose clock output pin for TX PLL1.
TXCLK_OUT2	Dual-purpose clock output pin for TX PLL2.
FAST[1..4]	Dedicated pins for driving the global fast lines within the entire device.
CLK1p	Dedicated global clock input.
CLK1n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK1p input.
CLK2p	Dedicated global clock input.
CLK2n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK2p input.
CLK3p	Dedicated global clock input.
CLK3n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK3p input.

Table 2. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
CLK4n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK4p input.
CLK5p	Dedicated global clock input.
CLK5n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK5p input.
CLK6p	Dedicated global clock input.
CLK6n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input for the CLK6p input.
CLK7p	Dedicated global clock input.
CLK7n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK7p input.
CLK8p	Dedicated global clock input.
CLK8n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK8p input.
Lock1	Dual-purpose pin for Lock output of general-purpose PLL1. If the PLL is not used, then this is a regular I/O pin.
Lock2	Dual-purpose pin for lock output of general-purpose PLL2. If the PLL is not used, then this is a regular I/O pin.
Lock3	Dual-purpose pin for lock output of general-purpose PLL3. If the PLL is not used, then this is a regular I/O pin.
Lock4	Dual-purpose pin for lock output of general-purpose PLL4. If the PLL is not used, then this is a regular I/O pin.
CLKLK_FB1	Dual-purpose external feedback pin for general-purpose PLL1.

Table 2. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
CLKLK_FB2	Dual-purpose external feedback pin for general-purpose PLL2.
CLKLK_OUT1	Dual-purpose external clock output pin for general-purpose PLL1.
CLKLK_OUT2	Dual-purpose external clock output pin for general-purpose PLL2.
VCCSEL	Dedicated input that is used to choose whether programming input pins can accept 3.3 V, 2.5 V, or 1.8V during configuration. A high (1.5 V, 1.8 V, 2.5 V, 3.3 V) means 1.8 V, and a "0" means 2.5 V/3.3 V.
VCCINT	Internal core voltage.
VCCIO[1..8]	I/O and configuration pin voltage. For I/O banks, these can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
VCC_CKLK[1..4]	Digital power for the four general-purpose PLLs.
VCC_CKLK[5,7]	Digital power for the high-speed receiver PLLs 1 and 2, respectively.
VCC_CKLK[6,8]	Digital power for the high-speed transmitter PLLs 1 and 2, respectively.
VCC_CKOUT[1,2]	External clock output buffer power for CLKLK_OUT1 and CLKLK_OUT2 of PLL1 and PLL2.
VREFC[1..8]	VREF control the circuit's dedicated power pin for each of the I/O banks. This pin can be connected to 2.5 V or 3.3V if a voltage referenced I/O standard is used. Otherwise, it can be connected to 1.8 V, 2.5 V, or 3.3 V.