Table 1 shows all pins for the EP2A70 724-pin ball-grid array (BGA) and 1,508-pin FineLine BGA packages.

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
8	IO	TrueDiff_TX01p	C25	E39	No
8	IO	TrueDiff_TX01n (2)	C24	E38	No
8	IO	TrueDiff_TX02n (2)	C27	F37	No
8	IO	TrueDiff_TX02p	C26	F36	No
-	VCCIO		VCCIO8	VCCIO8	
8	IO	TrueDiff_TX03p	D25	F39	No
8	IO	TrueDiff_TX03n (2)	D24	F38	No
8	IO	nWS (3)	J20	G30	
8	IO	TrueDiff_TX04n (2)	D27	G37	No
8	IO	TrueDiff_TX04p	D26	G36	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	TrueDiff_TX05p	E25	G39	No
8	IO	TrueDiff_TX05n (2)	E24	G38	No
8	IO	nRS (3)	J21	H31	
8	IO	TrueDiff_TX06n (2)	E27	H37	No
8	IO	TrueDiff_TX06p	E26	H36	No
-	GNDIO		GND	GND	
8	IO	TrueDiff_TX07p	F25	H39	No
8	IO	TrueDiff_TX07n (2)	F24	H38	No
8	IO	nCS (3)	K20	H30	
8	IO	TrueDiff_TX08n (2)	F27	J39	No
8	IO	TrueDiff_TX08p	F26	J38	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	TrueDiff_TX09p	G25	J37	No
8	IO	TrueDiff_TX09n (2)	G24	J36	No
8	IO	CS (3)	K21	H29	
8	IO	TrueDiff_TX10n (2)	G27	K39	No
8	IO	TrueDiff_TX10p	G26	K38	No
-	VCCIO		VCCIO8	VCCIO8	
8	IO	TrueDiff_TX11p	H25	K37	No
8	IO	TrueDiff_TX11n (2)	H24	K36	No
8	IO	DEV_CLRn (4)	K19	J30	
8	IO	TrueDiff_TX12n (2)	H27	L39	No
8	IO	TrueDiff_TX12p	H26	L38	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	TrueDiff_TX13p	J25	L37	No
8	IO	TrueDiff_TX13n (2)	J24	L36	No
8	IO		F23	G28	
8	IO	TrueDiff_TX14n (2)	J27	M39	No
8	IO	TrueDiff_TX14p	J26	M38	No
-	GNDIO		GND	GND	
8	IO	TrueDiff_TX15p	K25	M37	No
8	IO	TrueDiff_TX15n (2)	K24	M36	No
8	IO	TXLOCK1 (5)	L18	J29	
8	IO	TrueDiff_TX16n (2)	L25	N38	No
8	IO	TrueDiff_TX16p	L24	P39	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO	TrueDiff_TX17p	L27	P38	No
8	IO	TrueDiff_TX17n (2)	L26	R38	No

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
8	IO	LOCK4 (5)	L21	H28	
8	IO	TrueDiff_TX18n (2)	M27	T39	No
8	IO	TrueDiff_TX18p	M26	T38	No
-	VCCIO		VCCIO8	VCCIO8	
8	IO	TXCLK_OUT01p (6)	M25	U39	No
8	IO	TXCLK_OUT01n (2)	M24	U38	No
8	IO	DATA6 (3)	K22	H27	
8	IO		N27	V39	No
8	IO		N26	V38	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	K31	
8	IO		-	K30	
8	IO		G23	J28	
8	IO		-	J31	
8	IO		-	K29	
-	GNDIO		GND	GND	
8	IO		-	J33	
8	IO		-	L30	
8	IO		G22	J27	
8	IO		-	H33	
8	IO		-	K28	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	H35	
8	IO		-	J32	
8	IO		G20	J26	
8	IO		-	L31	
8	IO		-	L29	
-	VCCIO		VCCIO8	VCCIO8	
8	IO		-	J34	
8	IO		-	K27	
8	IO		G19	K26	
8	IO		-	J35	
8	IO		-	L28	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	L32	
8	IO		-	M30	
8	IO		G18	L27	
8	IO		-	K34	
8	IO		-	M29	
-	GNDIO		GND	GND	
8	IO		-	L33	
8	IO		-	M31	
8	IO		H22	L26	
8	IO		-	K35	
8	IO		-	M28	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	L35	
8	IO		-	M32	
8	IO		H21	L25	
8	IO		-	M33	
8	IO		-	M27	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
-	VCCIO		VCCIO8	VCCIO8	
8	IO		-	M34	
8	IO		-	N30	
8	IO		H23	M26	
8	IO		-	N31	
8	IO		-	N29	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	M35	
8	IO		-	N32	
8	IO		J22	N28	
8	IO		-	N34	
8	IO		-	P30	
-	VCCIO		VCCIO8	VCCIO8	
8	IO		-	P31	
8	IO		-	M25	
8	IO		H19	N27	
8	IO		-	N35	
8	IO		-	P29	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	N36	
8	IO		-	P32	
8	IO		J23	N26	
8	IO		-	P33	
8	IO		-	P28	
-	GNDIO		GND	GND	
8	IO		-	N37	
8	IO		-	N25	
8	IO		-	P27	
8	IO		-	P35	
8	IO		-	R30	
-	GNDIO		GND	GND	
8	IO		-	R31	
8	IO		-	P26	
8	IO		H18	R29	
8	IO		-	P36	
8	IO		-	P25	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	P37	
8	IO		-	R32	
8	IO		L20	R28	
8	IO		-	R34	
8	IO		-	R27	
-	VCCIO		VCCIO8	VCCIO8	
8	IO		-	R36	
8	IO		-	R35	
8	IO		N18	R26	
8	IO		-	R37	
8	IO		-	T30	
-	VCCINT		VCCINT	VCCINT	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
-	GNDINT		GND	GND	
8	IO		-	T32	
8	IO		-	T31	
8	IO		L22	T29	
8	IO		-	T33	
8	IO		-	R25	
-	GNDIO		GND	GND	
8	IO		-	T34	
8	IO		-	T28	
8	IO		M20	T27	
8	IO		-	T35	
8	IO		-	T26	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	T37	
8	IO		-	T36	
8	IO		N19	T25	
8	IO		-	U31	
8	IO		-	U27	
-	VCCIO		VCCIO8	VCCIO8	
8	IO		-	U33	
8	IO		-	U32	
8	IO		M21	U28	
8	IO		-	U34	
8	IO		-	U30	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	U35	
8	IO		-	U26	
8	IO		M22	U25	
8	IO		-	U36	
8	IO		-	V25	
-	GNDIO		GND	GND	
8	IO		-	V34	
8	IO		-	U37	
8	IO		M23	V27	
8	IO		-	V31	
8	IO		-	V30	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
8	IO		-	V33	
8	IO		-	V32	
8	IO		-	V28	
8	IO		-	V35	
8	IO		-	V26	
-	VCCIO		VCCIO8	VCCIO8	
8	IO	DATA7 (3)	L23	V37	
8	IO		-	V36	
8	IO		-	W25	
8	IO		-	W27	
8	IO		-	W26	
8	VREFC8 (7)		L19	W32	
-	GND_CKLK6 (8)		N21	U29	
-	VCC_CKLK6 (8)		M19	V29	
-	VCC_CKLK4 (8)		M18	W29	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
-	GND_CKLK4 (8)		N20	W28	
8	IO		-	W31	
8	IO		P23	W30	
8	IO		-	Y25	
8	IO		-	W34	
-	GNDIO		GND	GND	
8	IO	CLKLK_FB2n (2)	N25	W36	
9	CLKLK_FB2p (9), (10)		N24	W37	
8	IO	CLK4n (2)	N22	W38	
8	CLK4p		N23	W39	
8	IO	CLK2n (2)	P25	Y38	
-	VCCIO		VCCIO8	VCCIO8	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
-	nIO_PULLUP (9), (11)		P22	Y26	
8	DATA0 (9), (12)		P18	Y33	
8	DCLK (9)		P21	Y34	
8	CLK2p		P24	Y39	
8	nCE (9)		T23	AA26	
8	TDI (9)		T22	Y35	
-	GNDIO		GND	GND	
-	GND_CKLK2 (8)		P20	Y28	
-	GNDINT		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCC_CKLK2 (8)		P19	Y29	
-	VCCIO		VCCIO7	VCCIO7	
7	IO	DEV_OE (4)	R21	AA35	
-	VCC_CKOUT2 (13)		U23	AA29	
-	GND_CKOUT2 (13)		R18	AA28	
9	CLKLK_OUT2p (9), (14)		P27	Y37	
7	IO	CLKLK_OUT2n (2)	P26	Y36	
-	GNDIO		GND	GND	
7	IO	CLK6n (2)	R22	AA36	
7	CLK6p		R23	AA37	
7	IO	LOCK2 (5)	R19	AA30	
7	IO	CLK8n (2)	R24	AA38	
7	CLK8p		R25	AA39	
-	VCC_CKLKA (15)		U22	AA27	
-	VCC_CKLK8 (8)		T18	AB29	
-	VCCIO		VCCIO7	VCCIO7	
-	GND_CKLK8 (8)		R20	AC29	
7	VREFC7 (7)		T19	AB25	
7	IO		-	AA31	
7	IO		-	AA32	
7	IO		U18	AB26	
7	IO		-	AA33	
7	IO		-	AA34	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
-	GNDIO		GND	GND	
7	IO		-	AB27	
7	IO		-	AB37	
7	IO		T20	AB28	
7	IO		-	AB35	
7	IO		-	AB36	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AC25	
7	IO		-	AB34	
7	IO		U19	AC26	
7	IO		-	AB32	
7	IO		-	AB33	
-	VCCIO		VCCIO7	VCCIO7	
7	IO		-	AB30	
7	IO		-	AB31	
7	IO		T21	AC27	
7	IO		-	AC36	
7	IO		-	AC37	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AC28	
7	IO		-	AC35	
7	IO		U20	AD25	
7	IO		-	AC33	
7	IO		-	AC34	
-	GNDIO		GND	GND	
7	IO		-	AD26	
7	IO		-	AC32	
7	IO		V19	AD27	
7	IO		-	AC31	
7	IO		-	AD37	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AC30	
7	IO		-	AD36	
7	IO		U21	AE25	
7	IO		-	AD28	
7	IO		-	AD35	
-	VCCIO		VCCIO7	VCCIO7	
7	IO		-	AE26	
7	IO		-	AD34	
7	IO		V20	AE27	
7	IO		-	AD29	
7	IO		-	AD33	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AF25	
7	IO		-	AE37	
7	IO		W20	AF26	
7	IO		-	AD31	
7	IO		-	AE36	
-	GNDIO		GND	GND	
7	IO		-	AD30	
7	IO		-	AE35	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
7	IO		V21	AE28	
7	IO		-	AF37	
7	IO		-	AE34	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AG25	
7	IO		-	AF36	
7	IO		Y19	AF27	
7	IO		-	AE29	
7	IO		-	AE32	
-	VCCIO		VCCIO7	VCCIO7	
7	IO		-	AG26	
7	IO		-	AF34	
7	IO		-	AF28	
7	IO		-	AE30	
7	IO		-	AE31	
-	VCCIO		VCCIO7	VCCIO7	
7	IO		-	AH25	
7	IO		-	AG37	
7	IO		V22	AG27	
7	IO		-	AG35	
7	IO		-	AG36	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AH26	
7	IO		-	AF32	
7	IO		W21	AF29	
7	IO		-	AH35	
7	IO		-	AG34	
-	GNDIO		GND	GND	
7	IO		-	AJ25	
7	IO		-	AF31	
7	IO		W23	AG28	
7	IO		-	AF30	
7	IO		-	AG33	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCCIO		VCCIO7	VCCIO7	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AH27	
7	IO		-	AG32	
7	IO		AA19	AG29	
7	IO		-	AJ26	
7	IO		-	AH34	
-	GNDIO		GND	GND	
7	IO		-	AH28	
7	IO		-	AG31	
7	IO		Y23	AJ27	
7	IO		-	AG30	
7	IO		-	AH33	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AK26	
7	IO		-	AJ35	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
7	IO		Y21	AH29	
7	IO		-	AJ34	
7	IO		-	AH32	
-	VCCIO		VCCIO7	VCCIO7	
7	IO		-	AJ28	
7	IO		-	AK35	
7	IO		Y22	AK27	
7	IO		-	AK34	
7	IO		-	AH31	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AL26	
7	IO		-	AL35	
7	IO		AA20	AL27	
7	IO		-	AH30	
7	IO		-	AK33	
-	GNDIO		GND	GND	
7	IO		-	AJ29	
7	IO		-	AL34	
7	IO		AA23	AK28	
7	IO		-	AM33	
7	IO		-	AM35	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		-	AL28	
7	IO		-	AJ31	
7	IO		AA22	AM27	
7	IO		-	AL31	
7	IO		-	AK32	
-	VCCIO		VCCIO7	VCCIO7	
7	IO		-	AJ30	
7	IO		-	AK31	
7	IO		AB23	AK29	
7	IO		-	AM31	
7	IO		-	AL32	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO		R26	AB38	No
7	IO		R27	AB39	No
7	IO		-	AM28	
7	IO	TXCLK_OUT2n (2)	T24	AC38	No
7	IO	TXCLK_OUT2p (6)	T25	AC39	No
-	GNDIO		GND	GND	
7	IO	TrueDiff_TX36p	T26	AD38	No
7	IO	TrueDiff_TX36n (2)	T27	AD39	No
7	IO		-	AL29	
7	IO	TrueDiff_TX35n (2)	U26	AE38	No
7	IO	TrueDiff_TX35p	U27	AF38	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX34p	U24	AF39	No
7	IO	TrueDiff_TX34n (2)	U25	AG38	No
7	IO		-	AK30	
7	IO	TrueDiff_TX33n (2)	V24	AH36	No
7	IO	TrueDiff_TX33p	V25	AH37	No

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
-	VCCIO		VCCIO7	VCCIO7	
7	IO	TrueDiff_TX32p	W26	AH38	No
7	IO	TrueDiff_TX32n (2)	W27	AH39	No
7	IO		-	AN28	
7	IO	TrueDiff_TX31n (2)	W24	AJ36	No
7	IO	TrueDiff_TX31p	W25	AJ37	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX30p	Y26	AJ38	No
7	IO	TrueDiff_TX30n (2)	Y27	AJ39	No
7	IO	TXLOCK2 (10)	W22	AM29	
7	IO	TrueDiff_TX29n (2)	Y24	AK36	No
7	IO	TrueDiff_TX29p	Y25	AK37	No
-	GNDIO		GND	GND	
7	IO	TrueDiff_TX28p	AA26	AK38	No
7	IO	TrueDiff_TX28n (2)	AA27	AK39	No
7	IO		-	AL30	
7	IO	TrueDiff_TX27n (2)	AA24	AL38	No
7	IO	TrueDiff_TX27p	AA25	AL39	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX26p	AB26	AL36	No
7	IO	TrueDiff_TX26n (2)	AB27	AL37	No
7	IO		-	AN29	
7	IO	TrueDiff_TX25n (2)	AB24	AM38	No
7	IO	TrueDiff_TX25p	AB25	AM39	No
-	VCCIO		VCCIO7	VCCIO7	
7	IO	TrueDiff_TX24p	AC26	AM36	No
7	IO	TrueDiff_TX24n (2)	AC27	AM37	No
7	IO		-	AM30	
7	IO	TrueDiff_TX23n (2)	AC24	AN38	No
7	IO	TrueDiff_TX23p	AC25	AN39	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
7	IO	TrueDiff_TX22p	AD26	AN36	No
7	IO	TrueDiff_TX22n (2)	AD27	AN37	No
7	IO		-	AN30	
7	IO	TrueDiff_TX21n (2)	AD24	AP38	No
7	IO	TrueDiff_TX21p	AD25	AP39	No
-	GNDIO		GND	GND	
7	IO	TrueDiff_TX20p	AE26	AP36	No
7	IO	TrueDiff_TX20n (2)	AE27	AP37	No
7	IO	TrueDiff_TX19n (2)	AE24	AR38	No
7	IO	TrueDiff_TX19p	AE25	AR39	No
-	VCCIO		VCCIO7	VCCIO7	
6	IO	FlexDiff_TX01n (2)	AF25	AV36	
6	IO	FlexDiff_TX01p	AG25	AU36	
6	IO	FlexDiff_TX57n (2)	-	AR33	
6	IO	FlexDiff_TX57p	-	AP33	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX02n (2)	AG24	AR32	
6	IO	FlexDiff_TX02p	AF24	AP32	
6	IO	FlexDiff_TX58n (2)	-	AR31	
6	IO	FlexDiff_TX58p	-	AP31	
6	IO	FlexDiff_TX03n (2)	AD23	AR30	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
6	IO	FlexDiff_TX03p	AE23	AP30	
6	IO	FlexDiff_TX59n (2)	-	AU35	
6	IO	FlexDiff_TX59p	-	AT35	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX04n (2)	AG23	AW35	
6	IO	FlexDiff_TX04p	AF23	AV35	
6	IO	FlexDiff_TX60n (2)	-	AU34	
6	IO	FlexDiff_TX60p	-	AT34	
6	IO	FlexDiff_TX05n (2)	AB22	AW34	
6	IO	FlexDiff_TX05p	AC22	AV34	
6	IO	FlexDiff_TX06n (2)	AE22	AU33	
6	IO	FlexDiff_TX06p	AD22	AT33	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX07n (2)	AF22	AW33	
6	IO	FlexDiff_TX07p	AG22	AV33	
6	IO	FlexDiff_TX08n (2)	AC21	AU32	
6	IO	FlexDiff_TX08p	AB21	AT32	
6	IO	FlexDiff_TX09n (2)	AD21	AW32	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX09p	AE21	AV32	
6	IO	FlexDiff_TX10n (2)	AG21	AU31	
6	IO	FlexDiff_TX10p	AF21	AT31	
6	IO	FlexDiff_TX61n (2)	-	AW31	
6	IO	FlexDiff_TX61p	-	AV31	
6	IO	FlexDiff_TX11n (2)	AB20	AU30	
6	IO	FlexDiff_TX11p	AC20	AT30	
6	IO	FlexDiff_TX62n (2)	-	AR29	
6	IO	FlexDiff_TX62p	-	AP29	
6	IO	FlexDiff_TX12n (2)	AE20	AU29	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX12p	AD20	AT29	
6	IO	FlexDiff_TX63n (2)	-	AW30	
6	IO	FlexDiff_TX63p	-	AV30	
6	IO	FlexDiff_TX13n (2)	AF20	AR28	
6	IO	FlexDiff_TX13p	AG20	AP28	
6	IO	FlexDiff_TX64n (2)	-	AR27	
6	IO	FlexDiff_TX64p	-	AP27	
6	IO	FlexDiff_TX14n (2)	AC19	AR26	
6	IO	FlexDiff_TX14p	AB19	AP26	
6	IO		AA18	AN25	
6	IO		Y18	AN26	
6	VREFC6 (7)		Y17	AN27	
-	VCCIO		VCCIO6	VCCIO6	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
6	IO	CDS_ENA (16)	Y16	AN23	
6	IO		AA17	AN24	
6	IO	FlexDiff_TX15p	AD19	AR25	
6	IO	FlexDiff_TX15n (2)	AE19	AP25	
6	IO	FlexDiff_TX65p	-	AR24	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX65n (2)	-	AP24	
6	IO	FlexDiff_TX16p	AG19	AU28	
6	IO	FlexDiff_TX16n (2)	AF19	AT28	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
6	IO	FlexDiff_TX66p	-	AW29	
6	IO	FlexDiff_TX66n (2)	-	AV29	
6	IO	FlexDiff_TX17p	AC18	AW28	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX17n (2)	AB18	AV28	
6	IO	FlexDiff_TX67p	-	AU27	
6	IO	FlexDiff_TX67n (2)	-	AT27	
6	IO	FlexDiff_TX18p	AE18	AW26	
6	IO	FlexDiff_TX18n (2)	AD18	AV27	
6	IO	FlexDiff_TX68p	-	AU26	
6	IO	FlexDiff_TX68n (2)	-	AT26	
6	IO	FlexDiff_TX19p	AB17	AU25	
6	IO	FlexDiff_TX19n (2)	AC17	AT25	
6	IO	FlexDiff_TX20p	AE17	AV25	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX20n (2)	AD17	AV26	
6	IO	FlexDiff_TX21p	AF17	AU24	
6	IO	FlexDiff_TX21n (2)	AG17	AT24	
6	IO	FlexDiff_TX22p	AB16	AW24	
6	IO	FlexDiff_TX22n (2)	AC16	AV24	
6	IO	FlexDiff_TX23p	AD16	AR23	
6	IO	FlexDiff_TX23n (2)	AE16	AP23	
6	IO	FlexDiff_TX24p	AG16	AU23	
6	IO	FlexDiff_TX24n (2)	AF16	AT23	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX69p	-	AW23	
6	IO	FlexDiff_TX69n (2)	-	AV23	
6	IO	FlexDiff_TX25p	AB15	AR22	
6	IO	FlexDiff_TX25n (2)	AC15	AP22	
6	IO	FlexDiff_TX70p	-	AU22	
6	IO	FlexDiff_TX70n (2)	-	AT22	
-	VCCIO		VCCIO6	VCCIO6	
6	IO	FlexDiff_TX26p	AE15	AW22	
6	IO	FlexDiff_TX26n (2)	AD15	AV22	
6	IO	FlexDiff_TX71p	-	AU21	
6	IO	FlexDiff_TX71n (2)	-	AT21	
6	IO	FlexDiff_TX27p	AF15	AW21	
-	GNDIO		GND	GND	
6	IO	FlexDiff_TX27n (2)	AG15	AV21	
6	IO	FlexDiff_TX72p	-	AW20	
6	IO	FlexDiff_TX72n (2)	-	AV20	
6	IO	FlexDiff_TX28p	AG14	AR20	
6	IO	FlexDiff_TX28n (2)	AF14	AP20	
-	VCCIO		VCCIO6	VCCIO6	
-	VCCINT		VCCINT	VCCINT	
5	CONF_DONE (9)		AA15	AN20	
5	nSTATUS (9)		Y15	AN22	
5	FAST4 (17)		AA16	AP21	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
5	FAST3 (17)		AC14	AM21	
5	TCK (9)		Y14	AN18	
5	TMS (9)		AB14	AN19	
-	VCCIO		VCCIO5	VCCIO5	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
5	IO	FlexDiff_TX56n (2)	AD14	AT20	
5	IO	FlexDiff_TX56p	AE14	AU20	
5	IO	FlexDiff_TX73n (2)	-	AV19	
5	IO	FlexDiff_TX73p	-	AW19	
5	IO	FlexDiff_TX55n (2)	AF13	AT19	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX55p	AG13	AU19	
5	IO	FlexDiff_TX74n (2)	-	AP19	
5	IO	FlexDiff_TX74p	-	AR19	
5	IO	FlexDiff_TX54n (2)	AD13	AV18	
5	IO	FlexDiff_TX54p	AE13	AW18	
-	VCCIO		VCCIO5	VCCIO5	
5	IO	FlexDiff_TX75n (2)	-	AT18	
5	IO	FlexDiff_TX75p	-	AU18	
5	IO	FlexDiff_TX53n (2)	AB13	AP18	
5	IO	FlexDiff_TX53p	AC13	AR18	
5	IO	FlexDiff_TX76n (2)	-	AV17	
5	IO	FlexDiff_TX76p	-	AW17	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX52n (2)	AF12	AT17	
5	IO	FlexDiff_TX52p	AG12	AU17	
5	IO	FlexDiff_TX51n (2)	AD12	AP17	
5	IO	FlexDiff_TX51p	AE12	AR17	
5	IO	FlexDiff_TX50n (2)	AB12	AV16	
5	IO	FlexDiff_TX50p	AC12	AW16	
5	IO	FlexDiff_TX49n (2)	AF11	AT16	
5	IO	FlexDiff_TX49p	AG11	AU16	
5	IO	FlexDiff_TX48n (2)	AD11	AV14	
-	VCCIO		VCCIO5	VCCIO5	
5	IO	FlexDiff_TX48p	AE11	AV15	
5	IO	FlexDiff_TX47n (2)	AB11	AT15	
5	IO	FlexDiff_TX47p	AC11	AU15	
5	IO	FlexDiff_TX77n (2)	-	AT14	
5	IO	FlexDiff_TX77p	-	AU14	
5	IO	FlexDiff_TX46n (2)	AD10	AV13	
5	IO	FlexDiff_TX46p	AE10	AW14	
5	IO	FlexDiff_TX78n (2)	-	AT13	
5	IO	FlexDiff_TX78p	-	AU13	
5	IO	FlexDiff_TX45n (2)	AB10	AV12	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX45p	AC10	AW12	
5	IO	FlexDiff_TX79n (2)	-	AV11	
5	IO	FlexDiff_TX79p	-	AW11	
5	IO	FlexDiff_TX44n (2)	AF9	AT12	
5	IO	FlexDiff_TX44p	AG9	AU12	
5	IO	FlexDiff_TX80n (2)	-	AP16	
5	IO	FlexDiff_TX80p	-	AR16	
5	IO	FlexDiff_TX43n (2)	AD9	AP15	
5	IO	FlexDiff_TX43p	AE9	AR15	
5	IO		Y13	AN17	
5	IO		AA13	AN15	
-	VCCIO		VCCIO5	VCCIO5	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
5	VREFC5 (7)		AA12	AN16	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
-	VCCIO		VCCIO5	VCCIO5	
5	IO		AA11	AN13	
5	IO		Y12	AN14	
5	IO	FlexDiff_TX42p	AB9	AP14	
5	IO	FlexDiff_TX42n (2)	AC9	AR14	
5	IO	FlexDiff_TX81p	-	AP13	
5	IO	FlexDiff_TX81n (2)	-	AR13	
5	IO	FlexDiff_TX41p	AG8	AP12	
5	IO	FlexDiff_TX41n (2)	AF8	AR12	
5	IO	FlexDiff_TX82p	-	AV10	
5	IO	FlexDiff_TX82n (2)	-	AW10	
5	IO	FlexDiff_TX40p	AD8	AT11	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX40n (2)	AE8	AU11	
5	IO	FlexDiff_TX83p	-	AP11	
5	IO	FlexDiff_TX83n (2)	-	AR11	
5	IO	FlexDiff_TX39p	AC8	AT10	
5	IO	FlexDiff_TX39n (2)	AB8	AU10	
5	IO	FlexDiff_TX84p	-	AV9	
5	IO	FlexDiff_TX84n (2)	-	AW9	
5	IO	FlexDiff_TX38p	AF7	AT9	
5	IO	FlexDiff_TX38n (2)	AG7	AU9	
5	IO	FlexDiff_TX37p	AE7	AV8	
-	VCCIO		VCCIO5	VCCIO5	
5	IO	FlexDiff_TX37n (2)	AD7	AW8	
5	IO	FlexDiff_TX36p	AB7	AT8	
5	IO	FlexDiff_TX36n (2)	AC7	AU8	
5	IO	FlexDiff_TX35p	AG6	AV7	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX35n (2)	AF6	AW7	
5	IO	FlexDiff_TX34p	AD6	AT7	
5	IO	FlexDiff_TX34n (2)	AE6	AU7	
5	IO	FlexDiff_TX33p	AC6	AV6	
5	IO	FlexDiff_TX33n (2)	AB6	AW6	
5	IO	FlexDiff_TX85p	-	AT6	
5	IO	FlexDiff_TX85n (2)	-	AU6	
5	IO	FlexDiff_TX32p	AF5	AV5	
5	IO	FlexDiff_TX32n (2)	AG5	AW5	
-	VCCIO		VCCIO5	VCCIO5	
5	IO	FlexDiff_TX86p	-	AT5	
5	IO	FlexDiff_TX86n (2)	-	AU5	
5	IO	FlexDiff_TX31p	AE5	AP10	
5	IO	FlexDiff_TX31n (2)	AD5	AR10	
5	IO	FlexDiff_TX87p	-	AP9	
5	IO	FlexDiff_TX87n (2)	-	AR9	
5	IO	FlexDiff_TX30p	AF4	AP8	
5	IO	FlexDiff_TX30n (2)	AG4	AR8	
-	GNDIO		GND	GND	
5	IO	FlexDiff_TX88p	-	AP7	
5	IO	FlexDiff_TX88n (2)	-	AR7	
5	IO	FlexDiff_TX29p	AG3	AU4	
5	IO	FlexDiff_TX29n (2)	AF3	AV4	
-	VCCIO		VCCIO4	VCCIO4	
4	IO	TrueDiff_RX19p	AE3	AR1	No
4	IO	TrueDiff_RX19n (2)	AE4	AR2	No

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
4	IO	TrueDiff_RX20n (2)	AE1	AP3	No
4	IO	TrueDiff_RX20p	AE2	AP4	No
-	GNDIO		GND	GND	
4	IO	TrueDiff_RX21p	AD3	AP1	No
4	IO	TrueDiff_RX21n (2)	AD4	AP2	No
4	IO		-	AN10	
4	IO	TrueDiff_RX22n (2)	AD1	AN3	No
4	IO	TrueDiff_RX22p	AD2	AN4	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX23p	AC3	AN1	No
4	IO	TrueDiff_RX23n (2)	AC4	AN2	No
4	IO		-	AM10	
4	IO	TrueDiff_RX24n (2)	AC1	AM3	No
4	IO	TrueDiff_RX24p	AC2	AM4	No
-	VCCIO		VCCIO4	VCCIO4	
4	IO	TrueDiff_RX25p	AB3	AM1	No
4	IO	TrueDiff_RX25n (2)	AB4	AM2	No
4	IO		-	AN11	
4	IO	TrueDiff_RX26n (2)	AB1	AL3	No
4	IO	TrueDiff_RX26p	AB2	AL4	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX27p	AA3	AL1	No
4	IO	TrueDiff_RX27n (2)	AA4	AL2	No
4	IO		-	AL10	
4	IO	TrueDiff_RX28n (2)	AA1	AK1	No
4	IO	TrueDiff_RX28p	AA2	AK2	No
-	GNDIO		GND	GND	
4	IO	TrueDiff_RX29p	Y3	AK3	No
4	IO	TrueDiff_RX29n (2)	Y4	AK4	No
4	IO		-	AM11	
4	IO	TrueDiff_RX30n (2)	Y1	AJ1	No
4	IO	TrueDiff_RX30p	Y2	AJ2	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX31p	W3	AJ3	No
4	IO	TrueDiff_RX31n (2)	W4	AJ4	No
4	IO		-	AN12	
4	IO	TrueDiff_RX32n (2)	W1	AH1	No
4	IO	TrueDiff_RX32p	W2	AH2	No
-	VCCIO		VCCIO4	VCCIO4	
4	IO	TrueDiff_RX33p	V3	AG2	No
4	IO	TrueDiff_RX33n (2)	V4	AF1	No
4	IO		-	AK10	
4	IO	TrueDiff_RX34n (2)	U3	AF2	No
4	IO	TrueDiff_RX34p	U4	AE2	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO	TrueDiff_RX35p	U1	AD1	No
4	IO	TrueDiff_RX35n (2)	U2	AD2	No
4	IO		-	AL11	
4	IO	TrueDiff_RX36n (2)	T1	AC1	No
4	IO	TrueDiff_RX36p	T2	AC2	No
-	GNDIO		GND	GND	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
4	IO		-	AN8	
4	IO		-	AM9	
4	IO		-	AM12	
4	IO	RXCLK_IN2n (2)	R1	AB1	No
4	IO	RXCLK_IN2p	R2	AB2	No
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AL8	
4	IO		-	AL9	
4	IO		AB5	AL12	
4	IO		-	AK9	
4	IO		-	AK11	
-	VCCIO		VCCIO4	VCCIO4	
4	IO		-	AJ9	
4	IO		-	AJ10	
4	IO		AA6	AL13	
4	IO		-	AM7	
4	IO		-	AM13	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AN5	
4	IO		AA5	AK12	
4	IO		AA8	AJ11	
4	IO		-	AL7	
4	IO		-	AL14	
-	GNDIO		GND	GND	
4	IO		-	AL6	
4	IO		-	AH10	
4	IO		AA9	AK13	
4	IO		-	AJ8	
4	IO		-	AJ12	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AL5	
4	IO		Y6	AM5	
4	IO		Y7	AK14	
4	IO		-	AH9	
4	IO		-	AH11	
-	VCCIO		VCCIO4	VCCIO4	
4	IO		-	AJ7	
4	IO		-	AK6	
4	IO		AA10	AJ13	
4	IO		-	AK5	
4	IO		-	AH12	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AH8	
4	IO		Y5	AG10	
4	IO		Y9	AJ14	
4	IO		-	AJ6	
4	IO		-	AJ15	
-	GNDIO		GND	GND	
4	IO		-	AH7	
4	IO		-	AG9	
4	IO		Y10	AG11	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
4	IO		-	AJ5	
4	IO		-	AH13	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	VCCIO		VCCIO4	VCCIO4	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AG8	
4	IO		W6	AF10	
4	IO		W7	AG12	
4	IO		-	AF9	
4	IO		-	AH14	
-	GNDIO		GND	GND	
4	IO		-	AH6	
4	IO		-	AF11	
4	IO		W8	AG13	
4	IO		-	AG7	
4	IO		-	AH15	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AG6	
4	IO		-	AH5	
4	IO		Y11	AG14	
4	IO		-	AH4	
4	IO		-	AF12	
-	VCCIO		VCCIO4	VCCIO4	
4	IO		-	AG5	
4	IO		W5	AE10	
4	IO		V7	AG15	
4	IO		-	AF7	
4	IO		-	AF13	
-	VCCIO		VCCIO4	VCCIO4	
4	IO		-	AG4	
4	IO		-	AH3	
4	IO		V8	AE11	
4	IO		-	AF6	
4	IO		-	AF14	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AF5	
4	IO		U6	AG3	
4	IO		V9	AE12	
4	IO		-	AE7	
4	IO		-	AD10	
-	GNDIO		GND	GND	
4	IO		-	AD9	
4	IO		-	AF15	
4	IO		U7	AE13	
4	IO		-	AF4	
4	IO		-	AD11	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AF3	
4	IO		-	AE6	
4	IO		U8	AE14	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
4	IO		-	AD8	
4	IO		-	AD12	
-	VCCIO		VCCIO4	VCCIO4	
4	IO		-	AD7	
4	IO		-	AE5	
4	IO		U9	AE15	
4	IO		-	AE4	
4	IO		-	AC10	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AC9	
4	IO		U5	AE3	
4	IO		U10	AD13	
4	IO		-	AD6	
4	IO		-	AD14	
-	GNDIO		GND	GND	
4	IO		-	AC8	
4	IO		-	AD5	
4	IO		T7	AD15	
4	IO		-	AD4	
4	IO		-	AC12	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AD3	
4	IO		-	AC7	
4	IO		T8	AC13	
4	IO		-	AC6	
4	IO		-	AB10	
-	VCCIO		VCCIO4	VCCIO4	
4	IO		-	AB9	
4	IO		-	AC5	
4	IO		R7	AC14	
4	IO		-	AC4	
4	IO		-	AC15	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
4	IO		-	AC3	
4	IO		R6	AB8	
4	IO		R5	AB13	
4	IO		-	AB7	
4	IO		-	AB14	
-	GNDIO		GND	GND	
4	IO		-	AB5	
4	IO	RXLOCK2 (5)	V6	AB6	
4	IO		-	AB15	
4	IO		-	AB4	
4	IO		-	AA10	
4	VREFC4 (7)		T9	AA13	
-	GND_CKLK7 (8)		R8	AC11	
-	GND_CKLK7 (8)		T10	AB11	
-	VCCIO		VCCIO4	VCCIO4	
-	VCC_CKLK7 (8)		R9	AB12	
-	VCC_CKLKA (15)		T6	AA15	
4	IO		-	AB3	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
4	IO		-	AA9	
4	IO	LOCK1 (5)	T5	AA8	
4	IO		-	AA14	
4	IO		-	AA6	
-	VCC_CKLK1 (8)		R10	AA12	
-	GND_CKLK1 (8)		P8	AA11	
-	GNDIO		GND	GND	
4	IO	CLKLK_FB1n (2)	T3	AA4	
10	CLKLK_FB1p (9), (10)		T4	AA3	
4	IO	CLK3n (2)	R4	AA2	
4	CLK3p		R3	AA1	
4	IO	CLK1n (2)	P4	Y2	
-	VCCIO		VCCIO4	VCCIO4	
-	VCCINT		VCCINT	VCCINT	
-	GNDINT		GND	GND	
-	GNDIO		GND	GND	
4	nCONFIG (9)		P6	Y9	
4	PLL_ENA (9), (18)		P7	Y13	
-	VCCSEL (9), (19)		P5	Y6	
4	CLK1p		P3	Y1	
4	MSEL1 (9)		N5	Y7	
4	MSEL0 (9)		P9	Y15	
-	GNDIO		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCC_CKOUT1 (13)		P10	Y12	
-	GND_CKOUT1 (13)		N6	Y11	
10	CLKLK_OUT1p (9), (14)		P2	Y3	
3	IO	CLKLK_OUT1n (2)	P1	Y4	
-	VCC_CKLK3 (8)		N7	W12	
-	VCCIO		VCCIO3	VCCIO3	
-	GND_CKLK3 (8)		N8	W11	
3	IO		-	Y5	
3	IO	CLK5n (2)	N3	W4	
3	CLK5p		N4	W3	
3	IO	LOCK3 (5)	L6	W10	
3	IO		-	W9	
-	GNDIO		GND	GND	
-	GND_CKLK5 (8)		M7	V12	
-	GND_CKLK5 (8)		N9	U11	
-	VCC_CKLK5 (8)		N10	V11	
3	VREFC3 (7)		M10	W8	
3	IO	CLK7n (2)	M4	W2	
3	CLK7p		M3	W1	
3	IO		-	W14	
3	IO		-	W13	
3	IO		-	W7	
-	VCCIO		VCCIO3	VCCIO3	
3	IO		-	V10	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
3	IO		-	W6	
3	IO		M9	V13	
3	IO		M8	W15	
3	IO		-	W5	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	V15	
3	IO		-	V9	
3	IO		L10	V14	
3	IO		-	V8	
3	IO		-	V7	
-	GNDIO		GND	GND	
3	IO		-	U15	
3	IO		-	V6	
3	IO		M6	U14	
3	IO		-	V5	
3	IO		-	V4	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	U10	
3	IO		-	V3	
3	IO		M5	U13	
3	IO		-	U8	
3	IO		-	U6	
-	VCCIO		VCCIO3	VCCIO3	
3	IO		-	U12	
3	IO		-	U9	
3	IO		L9	T15	
3	IO		-	U7	
3	IO		-	U5	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	T14	
3	IO		-	U4	
3	IO		L8	T13	
3	IO		-	T3	
3	IO		-	U3	
-	GNDIO		GND	GND	
3	IO		-	T12	
3	IO		-	T4	
3	IO		L5	T11	
3	IO		-	T6	
3	IO		-	T5	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	T10	
3	IO		-	T9	
3	IO		K9	R15	
3	IO		-	T8	
3	IO		-	T7	
-	VCCIO		VCCIO3	VCCIO3	
3	IO		-	R14	
3	IO		-	R3	
3	IO		K8	R13	
3	IO		K7	R12	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
3	IO		-	R4	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	P15	
3	IO		-	R5	
3	IO		K6	R11	
3	IO		-	R8	
3	IO		-	R6	
-	GNDIO		GND	GND	
3	IO		-	R10	
3	IO		-	R9	
3	IO		J8	P14	
3	IO		-	P4	
3	IO		-	P3	
-	GNDIO		GND	GND	
3	IO		-	P13	
3	IO		-	P5	
3	IO		H10	P12	
3	IO		-	N3	
3	IO		-	P6	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	N15	
3	IO		-	P8	
3	IO		J5	P11	
3	IO		-	P9	
3	IO		-	N4	
-	VCCIO		VCCIO3	VCCIO3	
3	IO		-	P10	
3	IO		-	N5	
3	IO		J7	N14	
3	IO		J6	N13	
3	IO		-	N6	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	GNDIO		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	N12	
3	IO		-	N8	
3	IO		H9	N11	
3	IO		-	N10	
3	IO		-	N9	
-	VCCIO		VCCIO3	VCCIO3	
3	IO		-	M15	
3	IO		-	M3	
3	IO		H7	M14	
3	IO		H5	M7	
3	IO		-	M5	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	M13	
3	IO		-	M8	
3	IO		H6	M12	
3	IO		-	L15	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
3	IO		-	L5	
-	GNDIO		GND	GND	
3	IO		-	M11	
3	IO		-	M9	
3	IO		G9	L14	
3	IO		-	M10	
3	IO		-	L6	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	L13	
3	IO		-	L7	
3	IO		G8	L12	
3	IO		-	L8	
3	IO		-	K5	
-	VCCIO		VCCIO3	VCCIO3	
3	IO		-	K14	
3	IO		-	K6	
3	IO		G5	L11	
3	IO		-	L9	
3	IO		-	K7	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO		-	K13	
3	IO		-	J5	
3	IO		G6	K12	
3	IO		-	H5	
3	IO		-	J6	
-	GNDIO		GND	GND	
3	IO		-	L10	
3	IO		-	J8	
3	IO		F5	J13	
3	IO		-	K10	
3	IO		-	J7	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	RXCLK_IN1p	N2	V2	No
3	IO	RXCLK_IN1n (2)	N1	V1	No
3	IO		-	K11	
3	IO	RXLOCK1 (5)	L7	J9	
3	IO		-	H7	
-	VCCIO		VCCIO3	VCCIO3	
3	IO	TrueDiff_RX18p	M2	U2	No
3	IO	TrueDiff_RX18n (2)	M1	U1	No
3	IO		-	J12	
3	IO	TrueDiff_RX17n (2)	L2	T2	No
3	IO	TrueDiff_RX17p	L1	T1	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX16p	L4	R2	No
3	IO	TrueDiff_RX16n (2)	L3	P2	No
3	IO		-	J11	
3	IO	TrueDiff_RX15n (2)	K4	P1	No
3	IO	TrueDiff_RX15p	K3	N2	No
-	GNDIO		GND	GND	
3	IO	TrueDiff_RX14p	J2	M2	No

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
3	IO	TrueDiff_RX14n (2)	J1	M1	No
3	IO		-	H12	
3	IO	TrueDiff_RX13n (2)	J4	L4	No
3	IO	TrueDiff_RX13p	J3	L3	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX12p	H2	L2	No
3	IO	TrueDiff_RX12n (2)	H1	L1	No
3	IO		-	J10	
3	IO	TrueDiff_RX11n (2)	H4	K4	No
3	IO	TrueDiff_RX11p	H3	K3	No
-	VCCIO		VCCIO3	VCCIO3	
3	IO	TrueDiff_RX10p	G2	K2	No
3	IO	TrueDiff_RX10n (2)	G1	K1	No
3	IO		-	H11	
3	IO	TrueDiff_RX09n (2)	G4	J4	No
3	IO	TrueDiff_RX09p	G3	J3	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX08p	F2	J2	No
3	IO	TrueDiff_RX08n (2)	F1	J1	No
3	IO		-	H9	
3	IO	TrueDiff_RX07n (2)	F4	H2	No
3	IO	TrueDiff_RX07p	F3	H1	No
-	GNDIO		GND	GND	
3	IO	TrueDiff_RX06p	E2	H4	No
3	IO	TrueDiff_RX06n (2)	E1	H3	No
3	IO		-	H10	
3	IO	TrueDiff_RX05n (2)	E4	G2	No
3	IO	TrueDiff_RX05p	E3	G1	No
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
3	IO	TrueDiff_RX04p	D2	G4	No
3	IO	TrueDiff_RX04n (2)	D1	G3	No
3	IO		-	G10	
3	IO	TrueDiff_RX03n (2)	D4	F2	No
3	IO	TrueDiff_RX03p	D3	F1	No
-	VCCIO		VCCIO3	VCCIO3	
3	IO	TrueDiff_RX02p	C2	F4	No
3	IO	TrueDiff_RX02n (2)	C1	F3	No
3	IO	TrueDiff_RX01n (2)	C4	E2	No
3	IO	TrueDiff_RX01p	C3	E1	No
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX29n (2)	A3	B4	
2	IO	FlexDiff_RX29p	B3	C4	
2	IO	FlexDiff_RX57n (2)	-	E7	
2	IO	FlexDiff_RX57p	-	F7	
2	IO	FlexDiff_RX30n (2)	A4	E8	
2	IO	FlexDiff_RX30p	B4	F8	
2	IO	FlexDiff_RX58n (2)	-	E9	
2	IO	FlexDiff_RX58p	-	F9	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX31n (2)	C5	E10	
2	IO	FlexDiff_RX31p	D5	F10	
2	IO	FlexDiff_RX59n (2)	-	C5	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
2	IO	FlexDiff_RX59p	-	D5	
2	IO	FlexDiff_RX32n (2)	A5	A5	
2	IO	FlexDiff_RX32p	B5	B5	
2	IO	FlexDiff_RX60n (2)	-	C6	
2	IO	FlexDiff_RX60p	-	D6	
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX33n (2)	E6	B6	
2	IO	FlexDiff_RX33p	F6	A6	
2	IO	FlexDiff_RX34n (2)	C6	C7	
2	IO	FlexDiff_RX34p	D6	D7	
2	IO	FlexDiff_RX35n (2)	A6	A7	
2	IO	FlexDiff_RX35p	B6	B7	
2	IO	FlexDiff_RX36n (2)	E7	C8	
2	IO	FlexDiff_RX36p	F7	D8	
2	IO	FlexDiff_RX37n (2)	C7	A8	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX37p	D7	B8	
2	IO	FlexDiff_RX38n (2)	A7	C9	
2	IO	FlexDiff_RX38p	B7	D9	
2	IO	FlexDiff_RX61n (2)	-	A9	
2	IO	FlexDiff_RX61p	-	B9	
2	IO	FlexDiff_RX39n (2)	E8	C10	
2	IO	FlexDiff_RX39p	F8	D10	
2	IO	FlexDiff_RX62n (2)	-	E11	
2	IO	FlexDiff_RX62p	-	F11	
2	IO	FlexDiff_RX40n (2)	C8	C11	
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX40p	D8	D11	
2	IO	FlexDiff_RX63n (2)	-	A10	
2	IO	FlexDiff_RX63p	-	B10	
2	IO	FlexDiff_RX41n (2)	A8	E12	
2	IO	FlexDiff_RX41p	B8	F12	
2	IO	FlexDiff_RX64n (2)	-	E13	
2	IO	FlexDiff_RX64p	-	F13	
2	IO	FlexDiff_RX42n (2)	E9	E14	
2	IO	FlexDiff_RX42p	F9	F14	
2	IO		G11	G15	
2	IO		G10	G14	
2	VREFC2 (7)		H11	G13	
-	GNDIO		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
-	VCCIO		VCCIO2	VCCIO2	
2	IO		G12	G17	
2	IO		H12	G16	
2	IO	FlexDiff_RX43p	C9	E15	
2	IO	FlexDiff_RX43n (2)	D9	F15	
2	IO	FlexDiff_RX65p	-	E16	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX65n (2)	-	F16	
2	IO	FlexDiff_RX44p	A9	C12	
2	IO	FlexDiff_RX44n (2)	B9	D12	
2	IO	FlexDiff_RX66p	-	A11	
2	IO	FlexDiff_RX66n (2)	-	B11	
2	IO	FlexDiff_RX45p	E10	A12	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX45n (2)	F10	B12	
2	IO	FlexDiff_RX67p	-	C13	
2	IO	FlexDiff_RX67n (2)	-	D13	
2	IO	FlexDiff_RX46p	C10	A14	
2	IO	FlexDiff_RX46n (2)	D10	B13	
2	IO	FlexDiff_RX68p	-	C14	
2	IO	FlexDiff_RX68n (2)	-	D14	
2	IO	FlexDiff_RX47p	E11	C15	
2	IO	FlexDiff_RX47n (2)	F11	D15	
2	IO	FlexDiff_RX48p	C11	B15	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX48n (2)	D11	B14	
2	IO	FlexDiff_RX49p	A11	C16	
2	IO	FlexDiff_RX49n (2)	B11	D16	
2	IO	FlexDiff_RX50p	E12	A16	
2	IO	FlexDiff_RX50n (2)	F12	B16	
2	IO	FlexDiff_RX51p	C12	E17	
2	IO	FlexDiff_RX51n (2)	D12	F17	
2	IO	FlexDiff_RX52p	A12	C17	
2	IO	FlexDiff_RX52n (2)	B12	D17	
-	VCCIO		VCCIO2	VCCIO2	
2	IO	FlexDiff_RX69p	-	A17	
2	IO	FlexDiff_RX69n (2)	-	B17	
2	IO	FlexDiff_RX53p	E13	E18	
2	IO	FlexDiff_RX53n (2)	F13	F18	
2	IO	FlexDiff_RX70p	-	C18	
2	IO	FlexDiff_RX70n (2)	-	D18	
2	IO	FlexDiff_RX54p	C13	A18	
2	IO	FlexDiff_RX54n (2)	D13	B18	
-	GNDIO		GND	GND	
2	IO	FlexDiff_RX71p	-	C19	
2	IO	FlexDiff_RX71n (2)	-	D19	
2	IO	FlexDiff_RX55p	A13	A19	
2	IO	FlexDiff_RX55n (2)	B13	B19	
2	IO	FlexDiff_RX72p	-	A20	
2	IO	FlexDiff_RX72n (2)	-	B20	
2	IO	FlexDiff_RX56p	C14	E20	
2	IO	FlexDiff_RX56n (2)	D14	F20	
-	VCCIO		VCCIO2	VCCIO2	
-	GNDINT		GND	GND	
1	TRST (9)		H13	H19	
1	nCEO (9)		G13	F19	
1	FAST1 (17)		E14	G18	
-	VCCINT		VCCINT	VCCINT	
-	VCCIO		VCCIO1	VCCIO1	
1	FAST2 (17)		H14	G21	
1	TDO (9)		F14	G22	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX28n (2)	B14	D20	
1	IO	FlexDiff_RX28p	A14	C20	
1	IO	FlexDiff_RX73n (2)	-	B21	
1	IO	FlexDiff_RX73p	-	A21	
1	IO	INIT_DONE/FlexDiff_RX27n (2), (3)	B15	D21	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
-	VCCIO		VCCIO1	VCCIO1	
1	IO	FlexDiff_RX27p	A15	C21	
1	IO	FlexDiff_RX74n (2)	-	F21	
1	IO	FlexDiff_RX74p	-	E21	
1	IO	FlexDiff_RX26n (2)	D15	B22	
1	IO	RDYnBSY/FlexDiff_RX26p (3)	C15	A22	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX75n (2)	-	D22	
1	IO	FlexDiff_RX75p	-	C22	
1	IO	FlexDiff_RX25n (2)	F15	F22	
1	IO	FlexDiff_RX25p	E15	E22	
1	IO	FlexDiff_RX76n (2)	-	B23	
1	IO	FlexDiff_RX76p	-	A23	
-	VCCIO		VCCIO1	VCCIO1	
1	IO	CLKUSR/FlexDiff_RX24n (2), (3)	B16	D23	
1	IO	FlexDiff_RX24p	A16	C23	
1	IO	FlexDiff_RX23n (2)	D16	F23	
1	IO	FlexDiff_RX23p	C16	E23	
1	IO	FlexDiff_RX22n (2)	F16	B24	
1	IO	DATA1 / FlexDiff_RX22p (3)	E16	A24	
1	IO	FlexDiff_RX21n (2)	B17	D24	
1	IO	FlexDiff_RX21p	A17	C24	
1	IO	FlexDiff_RX20n (2)	D17	B26	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX20p	C17	B25	
1	IO	FlexDiff_RX19n (2)	F17	D25	
1	IO	FlexDiff_RX19p	E17	C25	
1	IO	FlexDiff_RX77n (2)	-	D26	
1	IO	FlexDiff_RX77p	-	C26	
1	IO	FlexDiff_RX18n (2)	D18	B27	
1	IO	FlexDiff_RX18p	C18	A26	
1	IO	FlexDiff_RX78n (2)	-	D27	
1	IO	FlexDiff_RX78p	-	C27	
1	IO	FlexDiff_RX17n (2)	F18	B28	
-	VCCIO		VCCIO1	VCCIO1	
1	IO	FlexDiff_RX17p	E18	A28	
1	IO	FlexDiff_RX79n (2)	-	B29	
1	IO	FlexDiff_RX79p	-	A29	
1	IO	FlexDiff_RX16n (2)	B19	D28	
1	IO	FlexDiff_RX16p	A19	C28	
1	IO	FlexDiff_RX80n (2)	-	F24	
1	IO	FlexDiff_RX80p	-	E24	
1	IO	FlexDiff_RX15n (2)	D19	F25	
1	IO	FlexDiff_RX15p	C19	E25	
1	IO		G16	G23	
1	IO	DATA2 (3)	H15	G25	
-	GNDIO		GND	GND	
-	GNDINT		GND	GND	
-	VCCINT		VCCINT	VCCINT	
1	VREFC1 (7)		H17	G24	
-	VCCIO		VCCIO1	VCCIO1	
1	IO		G17	G27	
1	IO		H16	G26	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
1	IO	DATA3/FlexDiff_RX14p (3)	F19	F26	
1	IO	FlexDiff_RX14n (2)	E19	E26	
1	IO	FlexDiff_RX81p	-	F27	
1	IO	FlexDiff_RX81n (2)	-	E27	
1	IO	FlexDiff_RX13p	B20	F28	
1	IO	FlexDiff_RX13n (2)	A20	E28	
1	IO	FlexDiff_RX82p	-	B30	
1	IO	FlexDiff_RX82n (2)	-	A30	
1	IO	FlexDiff_RX12p	D20	D29	
-	VCCIO		VCCIO1	VCCIO1	
1	IO	FlexDiff_RX12n (2)	C20	C29	
1	IO	FlexDiff_RX83p	-	F29	
1	IO	FlexDiff_RX83n (2)	-	E29	
1	IO	FlexDiff_RX11p	F20	D30	
1	IO	FlexDiff_RX11n (2)	E20	C30	
1	IO	FlexDiff_RX84p	-	B31	
1	IO	FlexDiff_RX84n (2)	-	A31	
1	IO	FlexDiff_RX10p	B21	D31	
1	IO	FlexDiff_RX10n (2)	A21	C31	
1	IO	FlexDiff_RX09p	D21	B32	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX09n (2)	C21	A32	
1	IO	FlexDiff_RX08p	F21	D32	
1	IO	FlexDiff_RX08n (2)	E21	C32	
1	IO	FlexDiff_RX07p	B22	B33	
1	IO	FlexDiff_RX07n (2)	A22	A33	
1	IO	FlexDiff_RX06p	D22	D33	
1	IO	FlexDiff_RX06n (2)	C22	C33	
1	IO	FlexDiff_RX05p	F22	B34	
1	IO	FlexDiff_RX05n (2)	E22	A34	
-	VCCIO		VCCIO1	VCCIO1	
1	IO	FlexDiff_RX85p	-	D34	
1	IO	FlexDiff_RX85n (2)	-	C34	
1	IO	FlexDiff_RX04p	B23	B35	
1	IO	FlexDiff_RX04n (2)	A23	A35	
1	IO	FlexDiff_RX86p	-	D35	
1	IO	FlexDiff_RX86n (2)	-	C35	
1	IO	FlexDiff_RX03p	D23	F30	
1	IO	DATA5/ FlexDiff_RX03n (2), (3)	C23	E30	
-	GNDIO		GND	GND	
1	IO	FlexDiff_RX87p	-	F31	
1	IO	FlexDiff_RX87n (2)	-	E31	
1	IO	FlexDiff_RX02p	B24	F32	
1	IO	FlexDiff_RX02n (2)	A24	E32	
1	IO	FlexDiff_RX88p	-	F33	
1	IO	FlexDiff_RX88n (2)	-	E33	
1	IO	FlexDiff_RX01p	B25	C36	
1	IO	DATA4 /FlexDiff_RX01n (2), (3)	A25	B36	
-	VCCIO		VCCIO1	VCCIO1	
	VCCINT		L11	L16	
	VCCINT		L13	N16	
	VCCINT		L15	AG16	
	VCCINT		L17	AJ16	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
	VCCINT		V18	L24	
	VCCINT		J18	N24	
	VCCINT		J12	AG24	
	VCCINT		W16	AJ24	
	VCCINT		K11	M17	
	VCCINT		M12	P17	
	VCCINT		M14	T17	
	VCCINT		M16	V17	
	VCCINT		K17	Y17	
	VCCINT		K13	AB17	
	VCCINT		N13	AD17	
	VCCINT		N15	AF17	
	VCCINT		V13	AH17	
	VCCINT		W10	M23	
	VCCINT		J10	P23	
	VCCINT		P12	T23	
	VCCINT		P16	V23	
	VCCINT		W18	Y23	
	VCCINT		K15	AB23	
	VCCINT		R13	AD23	
	VCCINT		R15	AF23	
	VCCINT		V15	AH23	
	VCCINT		V11	N18	
	VCCINT		T12	R18	
	VCCINT		T14	U18	
	VCCINT		T16	W18	
	VCCINT		V17	AA18	
	VCCINT		U17	AC18	
	VCCINT		U11	AE18	
	VCCINT		U13	AG18	
	VCCINT		U15	N22	
	VCCINT			R22	
	VCCINT			U22	
	VCCINT			W22	
	VCCINT			AA22	
	VCCINT			AC22	
	VCCINT			AE22	
	VCCINT			AG22	
	VCCINT			M19	
	VCCINT			P19	
	VCCINT			T19	
	VCCINT			M21	
	VCCINT			P21	
	VCCINT			T21	
	VCCINT			AD21	
	VCCINT			AF21	
	VCCINT			AH21	
	VCCINT			AH19	
	VCCINT			AF19	
	VCCINT			AD19	
	VCCINT			M20	
	VCCINT			N20	
	VCCINT			P20	
	VCCINT			R20	
	VCCINT			U20	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
	VCCINT			V19	
	VCCINT			V21	
	VCCINT			AB21	
	VCCINT			AB19	
	VCCINT			AC20	
	VCCINT			AE20	
	VCCINT			AF20	
	VCCINT			AG20	
	VCCINT			AH20	
	VCCIO8		B27	D39	
	VCCIO8		K26	R39	
	VCCIO8		N17	W35	
	VCCIO8		K18	H32	
	VCCIO8			W24	
	VCCIO8			U24	
	VCCIO8			R24	
	VCCIO7		AF27	AA24	
	VCCIO7		R17	AC24	
	VCCIO7		V26	AE24	
	VCCIO7		W19	Y32	
	VCCIO7			AE39	
	VCCIO7			AT39	
	VCCIO7			AM32	
	VCCIO6		AF18	AJ21	
	VCCIO6		AG26	AJ22	
	VCCIO6		W15	AJ23	
	VCCIO6		Y20	AR21	
	VCCIO6			AW25	
	VCCIO6			AW36	
	VCCIO6			AN31	
	VCCIO5		AF10	AJ19	
	VCCIO5		AG2	AJ18	
	VCCIO5		W13	AJ17	
	VCCIO5		Y8	AN9	
	VCCIO5			AW4	
	VCCIO5			AW15	
	VCCIO5			AM20	
	VCCIO4		AF1	AT1	
	VCCIO4		R11	AE1	
	VCCIO4		V2	AA16	
	VCCIO4		V10	AC16	
	VCCIO4			AE16	
	VCCIO4			AM8	
	VCCIO4			AA5	
	VCCIO3		B1	W16	
	VCCIO3		K2	U16	
	VCCIO3		N11	R16	
	VCCIO3		K10	Y8	
	VCCIO3			R1	
	VCCIO3			D1	
	VCCIO3			H8	
	VCCIO2		A2	A4	
	VCCIO2		B10	A15	
	VCCIO2		J13	L19	
	VCCIO2		H8	L18	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
	VCCIO2			L17	
	VCCIO2			E19	
	VCCIO2			G9	
	VCCIO1		A26	L21	
	VCCIO1		B18	L22	
	VCCIO1		J15	L23	
	VCCIO1		H20	H20	
	VCCIO1			A25	
	VCCIO1			A36	
	VCCIO1			G31	
	GND		G15	G20	
	GND		J14	M24	
	GND		J16	P24	
	GND		K12	T24	
	GND		L12	V24	
	GND		L14	AB24	
	GND		L16	AD24	
	GND		K16	AF24	
	GND		W12	AH24	
	GND		M11	M16	
	GND		M13	P16	
	GND		M15	T16	
	GND		M17	V16	
	GND		W14	AB16	
	GND		J11	AD16	
	GND		N12	AF16	
	GND		N16	AH16	
	GND		J17	N17	
	GND		K14	R17	
	GND		P11	U17	
	GND		P17	W17	
	GND		V14	AA17	
	GND		W11	AC17	
	GND		R12	AE17	
	GND		R16	AG17	
	GND		W17	N23	
	GND		J9	R23	
	GND		T11	U23	
	GND		T13	W23	
	GND		T15	AA23	
	GND		T17	AC23	
	GND		V16	AE23	
	GND		V12	AG23	
	GND		U12	M18	
	GND		U14	P18	
	GND		U16	T18	
	GND			V18	
	GND			Y18	
	GND			AB18	
	GND			AD18	
	GND			AF18	
	GND			AH18	
	GND			M22	
	GND			P22	
	GND			T22	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
	GND			V22	
	GND			Y22	
	GND			AB22	
	GND			AD22	
	GND			AF22	
	GND			AH22	
	GND			N19	
	GND			R19	
	GND			U19	
	GND			N21	
	GND			R21	
	GND			U21	
	GND			AC21	
	GND			AE21	
	GND			AG21	
	GND			AC19	
	GND			AE19	
	GND			AG19	
	GND			L20	
	GND			AJ20	
	GND			V20	
	GND			AB20	
	GND			AD20	
	GND			T20	
	GND		A1	AW38	
	GND		A10	AW37	
	GND		A18	AV39	
	GND		A27	AU39	
	GND		B2	A37	
	GND		B26	A38	
	GND		E5	B39	
	GND		E23	C39	
	GND		G14	B38	
	GND		K1	AV38	
	GND		K5	A2	
	GND		K23	A3	
	GND		K27	B1	
	GND		V1	C1	
	GND		V5	B2	
	GND		V23	AV1	
	GND		V27	AU1	
	GND		AA14	AV2	
	GND		AC5	AW2	
	GND		AC23	AW3	
	GND		AF2	AW27	
	GND		AF26	A27	
	GND		AG1	AW13	
	GND		AG10	A13	
	GND		AG18	AG39	
	GND		AG27	N39	
	GND		AA7	N1	
	GND		AA21	AG1	
	GND		G7	AN21	
	GND		G21	AK20	
	GND		W9	W33	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
	GND		J19	Y30	
	GND			G19	
	GND			K20	
	GND			Y10	
	GND			AA7	
	GND			AU37	
	GND			AT36	
	GND			AR35	
	GND			AP34	
	GND			AN33	
	GND			C37	
	GND			D36	
	GND			E35	
	GND			F34	
	GND			G33	
	GND			C3	
	GND			D4	
	GND			E5	
	GND			F6	
	GND			G7	
	GND			AU3	
	GND			AT4	
	GND			AR5	
	GND			AP6	
	GND			AN7	
	NC			AA25	
	NC			AD32	
	NC			AE33	
	NC			AE8	
	NC			AE9	
	NC			AF33	
	NC			AF35	
	NC			AF8	
	NC			AJ32	
	NC			AJ33	
	NC			AK15	
	NC			AK16	
	NC			AK17	
	NC			AK18	
	NC			AK19	
	NC			AK21	
	NC			AK22	
	NC			AK23	
	NC			AK24	
	NC			AK25	
	NC			AK7	
	NC			AK8	
	NC			AL15	
	NC			AL16	
	NC			AL17	
	NC			AL18	
	NC			AL19	
	NC			AL20	
	NC			AL21	
	NC			AL22	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
	NC			AL23	
	NC			AL24	
	NC			AL25	
	NC			AL33	
	NC			AM14	
	NC			AM15	
	NC			AM16	
	NC			AM17	
	NC			AM18	
	NC			AM19	
	NC			AM22	
	NC			AM23	
	NC			AM24	
	NC			AM25	
	NC			AM26	
	NC			AM34	
	NC			AM6	
	NC			AN32	
	NC			AN34	
	NC			AN35	
	NC			AN6	
	NC			AP35	
	NC			AP5	
	NC			AR3	
	NC			AR34	
	NC			AR36	
	NC			AR37	
	NC			AR4	
	NC			AR6	
	NC			AT2	
	NC			AT3	
	NC			AT37	
	NC			AT38	
	NC			AU2	
	NC			AU38	
	NC			AV3	
	NC			AV37	
	NC			B3	
	NC			B37	
	NC			C2	
	NC			C38	
	NC			D2	
	NC			D3	
	NC			D37	
	NC			D38	
	NC			E3	
	NC			E34	
	NC			E36	
	NC			E37	
	NC			E4	
	NC			E6	
	NC			F35	
	NC			F5	
	NC			G11	
	NC			G12	

Table 1. EP2A70 Device Pin-Outs					
I/O & VREF Bank	**Pin Name/Function**	**Dual-Purpose Function**	**724-Pin BGA**	**1,508-Pin FinLine BGA**	**HSTL Class II Output Support (1)**
	NC			G29	
	NC			G32	
	NC			G34	
	NC			G35	
	NC			G5	
	NC			G6	
	NC			G8	
	NC			H13	
	NC			H14	
	NC			H15	
	NC			H16	
	NC			H17	
	NC			H18	
	NC			H21	
	NC			H22	
	NC			H23	
	NC			H24	
	NC			H25	
	NC			H26	
	NC			H34	
	NC			H6	
	NC			J14	
	NC			J15	
	NC			J16	
	NC			J17	
	NC			J18	
	NC			J19	
	NC			J20	
	NC			J21	
	NC			J22	
	NC			J23	
	NC			J24	
	NC			J25	
	NC			K15	
	NC			K16	
	NC			K17	
	NC			K18	
	NC			K19	
	NC			K21	
	NC			K22	
	NC			K23	
	NC			K24	
	NC			K25	
	NC			K32	
	NC			K33	
	NC			K8	
	NC			K9	
	NC			L34	
	NC			M4	
	NC			M6	
	NC			N33	
	NC			N7	
	NC			P34	
	NC			P7	
	NC			R33	

Table 1. EP2A70 Device Pin-Outs

I/O & VREF Bank	Pin Name/Function	Dual-Purpose Function	724-Pin BGA	1,508-Pin FinLine BGA	HSTL Class II Output Support (1)
	NC			R7	
	NC			Y14	
	NC			Y16	
	NC			Y24	
	NC			Y27	
	NC			Y31	
Total User I/O Pins (20)			536	1,060	

Notes:

(1) The pins marked "no" in this column do not support the HSTL Class II output standard. All the unmarked pins support HSTL class II output in addition to other I/O standards.

(2) This pin is the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the differential channel. Pins with "p" suffix carry the positive signal for the differential channel.

(3) This pin can be used as a user I/O pin after configuration.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remians high if a periodic clock remains clocking. The LOCK function is optional, if the LOCK output is not used, this pin is a user I/O pin.

(6) Dedicated external clock output from one of the two LVDS transmitter PLLs. TXCLK_OUT1p is from TXPLL1, TXCLK_OUT2p is from TXPLL2.

(7) This pin is the dedicated power pin of VREF Control circuits (In addition to the programmable VREF pins) for each of the I/O banks. This pin can be connected to 2.5 V or 3.3 V if a voltage referenced I/O standard is used. Otherwise, it can be connected to 1.8 V, 2.5 V, or 3.3 V.

(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To insure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as VCCINT and should be connected to a 1.5-V power supply. If the ClockLock and ClockBoost circuitry is not used, this power or ground pin should be connected to the VCCINT or GND, respectively.

(9) This pin is a dedicted pin; it is not available as a user I/O pin.

(10) Dedicated external clock feedback from the general-purpose PLLs. CLKLK_FB1p feeds PLL1, CLKLK_FB2p feeds PLL2. The external clock feedback must use the same I/O standard as the external clock output and the global clock input to the general-purpose PLL. If this pin feature is not used, it should be connected to GND on the board.

(11) Dedicated input that is used to control whether weak active pull-up resistors are on for all I/O pins during power-up and configuration. A "0" means active pull-up resistors are enabled, a "1" (1.5 V, 1.8 V, 2.5 V, 3.3 V) means they are disabled.

(12) This pin is tri-stated in user mode.

(13) This pin is power or ground (Bank #9 and #10 in the Quartus II software) for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock output. To insure noise resistance, the power and ground supply to the PLL external output should be isolated from power and ground to the rest of the device. If the PLL or external output is not used, this power and ground pin should be connected to VCCIO or GND respectively.

(14) Dedicated external clock output from the general-purpose PLLs. CLKLK_OUT1p is from PLL1, CLKLK_OUT2p is from PLL2. Each dedicated clock output has its own VCCIO power for output standard selection. If this pin feature is not used, it should be connected to GND on the board.

(15) This pin is a dedicated power pin for the ClockLock and ClockBoost circuitry. It should be connected to the highest voltage level on the device. If possible, do not connect this pin to a noisy VCCIO pin.

(16) This is a dual-purpose pin for enabling the clock data synchronization (CDS) circuitry.

(17) This pin is a dedicated pin for driving the global fast lines within the entire device.

(18) This pin is a dedicated input pin that is the active high enable pin for all of the PLL circuits in the device. When de-asserted (low), all PLLs are reset to their default unlocked state and will stop clocking. Once re-asserted (can be 1.5 V, 1.8 V, 2.5 V, 3.3 V but should be the same as the VCCIO for that bank), the PLLs will lock again and start clocking. This PLL enable control can be selected on a per PLL basis. If this pin feature is not used, it should be connected to GND on the board.

(19) Dedicated input that is used to choose whether programming input pins can accept 3.3 V, 2.5 V, or 1.8 V during configuration. A high (1.5 V, 1.8 V, 2.5 V, 3.3 V) means 1.8 V, and a "0" means 2.5 V/3.3 V.

(20) The user I/O pin count inclues 4 dedicated inputs and 8 dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Table 2 provides descriptions for all power, HSDI, and general-purpose PLL related pins.

Table 2. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
TrueDiff_RX[1..36]	Dual-purpose HSDI reciever channels 1 through 36. If not used, these pins are regular I/O pins.
TrueDiff_TX[1..36]	Dual-purpose HSDI transmitter channels 1 through 36. If not used, these pins are regular I/O pins.
FlexDiff_RX[1..88]	Dual-purpose Flexible-LVDS reciever channels 1 through 56. If not used, these pins are regular I/O pins.
FlexDiff_TX[1..88]	Dual-purpose Flexible-LVDS transmitter channels 1 through 56. If not used, these pins are regular I/O pins.
RXLOCK1	Dual-purpose pin for lock output of RX PLL1. If the PLL is not used, then this is a regular I/O pin.
RXLOCK2	Dual-purpose pin for lock output of RX PLL2. If the PLL is not used, then this is a regular I/O pin.
TXLOCK1	Dual-purpose pin for lock output of TX PLL1. If the PLL is not used, then this is a regular I/O pin.
TXLOCK2	Dual-purpose pin for lock output of TX PLL2. If the PLL is not used, then this is a regular I/O pin.
RXCLK IN1	Dual-purpose clock input pin for RX PLL1.
RXCLK IN2	Dual-purpose clock input pin for RX PLL2.
TXCLK OUT1	Dual-purpose clock output pin for TX PLL1.
TXCLK OUT2	Dual-purpose clock output pin for TX PLL2.
FAST[1..4]	Dedicated pins for driving the global fast lines within the entire device.
CLK1p	Dedicated global clock input.
CLK1n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK1p input.
CLK2p	Dedicated global clock input.
CLK2n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK2p input.
CLK3p	Dedicated global clock input.
CLK3n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK3p input.
CLK4p	Dedicated global clock input.
CLK4n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK4p input.
CLK5p	Dedicated global clock input.
CLK5n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK5p input.
CLK6p	Dedicated global clock input.
CLK6n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input for the
CLK7p	Dedicated global clock input.
CLK7n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK7p input.
CLK8p	Dedicated global clock input.
CLK8n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin can be used as the VREF input for the CLK8p input.
Lock1	Dual-purpose pin for Lock output of general-purpose PLL1. If the PLL is not used, then this is a regular I/O pin.

Table 2. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
Lock2	Dual-purpose pin for lock output of general-purpose PLL2. If the PLL is not used, then this is a regular I/O pin.
Lock3	Dual-purpose pin for lock output of general-purpose PLL3. If the PLL is not used, then this is a regular I/O pin.
Lock4	Dual-purpose pin for lock output of general-purpose PLL4. If the PLL is not used, then this is a regular I/O pin.
CLKLK FB1	Dual-purpose external feedback pin for general-purpose PLL1.
CLKLK FB2	Dual-purpose external feedback pin for general-purpose PLL2.
CLKLK OUT1	Dual-purpose external clock output pin for general-purpose PLL1.
CLKLK OUT2	Dual-purpose external clock output pin for general-purpose PLL2.
VCCSEL	Dedicated input that is used to choose whether programming input pins can accept 3.3 V, 2.5 V, or 1.8V during configuration. A high (1.5 V, 1.8 V, 2.5 V, 3.3 V) means 1.8 V, and a "0" means 2.5 V/3.3 V.
VCCINT	Internal core voltage.
VCCIO[1..8]	I/O and configuration pin voltage. For I/O banks, these can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
VCC CKLK[1..4]	Digital power for the four general-purpose PLLs.
VCC CKLK[5,7]	Digital power for the high-speed receiver PLLs 1 and 2, respectively.
VCC CKLK[6,8]	Digital power for the high-speed transmitter PLLs 1 and 2, respectively.
VCC_CKOUT[1,2]	External clock output buffer power for CLKLK_OUT1 and CLKLK_OUT2 of PLL1 and
VREFC[1..8]	VREF control the circuit's dedicated power pin for each of the I/O banks. This pin can be connected to 2.5 V or 3.3V if a voltage referenced I/O standard is used. Otherwise, it can be connected to 1.8 V, 2.5 V, or 3.3 V.