Pin Name	Pin Type	Description	88- Pin Ultra FineLine BGA
EXCLK	Input	External clock source	H3
DCLK	Output	Configuration device drive this signal to PLD as configuration clock	A10
DATA0	Output	PLD configuration output data bus	G12
DATA1	Output	PLD configuration output data bus	F11
DATA2	Output	PLD configuration output data bus	E11
DATA3	Output	PLD configuration output data bus	D11
DATA4	Output	PLD configuration output data bus	C11
DATA5	Output	PLD configuration output data bus	B11
DATA6	Output	PLD configuration output data bus	B12
DATA7	Output	PLD configuration output data bus	A11
OE	Open-Drain Input/Output	Configuration device sense OE goes high, before starting PLD configuration	B1
n INIT _ CONF	Output	Initiate configuration	C5
nCS	Input	Connected to CONF-DONE in PLD. PLD will drive it low, when OE asserted	G2
TDI	Input	JTAG data input	D2
TDO	Output	JTAG data output	E2
TMS	Input	JTAG mode selection	F2
TCK	Input	JTAG clock	C2
PGM1	Input	Select one of eight pages that contains configuration data	C6
PGM0	Input	Select one of eight pages that contains configuration data	B8
PGM2	Input	Select one of eight pages that contains configuration data	F5
PORSEL	Input	Select 2ms or 100ms POR	F6
TM0	Input	Select test mode for configuration device	H10
TM1	Input	Select test mode for configuration device	D5
GND	Supply	Ground pins	H2, G11, H11, A9, D3, H8
NC	No Connect	No Connect Pins	A1, A12, F3, F4, H1, H12
VCC	Supply	Power Supply Pins	G1, E7, G10, D6, A2, D9, D10
VCCW	Supply	Flash Program/Erase Power Supply	E4
C -WE#	Input	Controller write enable pin. Should be connected to F-WE# on the board.	B2
F -WE#	Input	Flash write enable pin. Should be connected to C-WE# on the board	C3
CE#	Input	Flash pin that activates the Flash memory	H7
OE#	Input	Flash pin that enable the drivers of Flash output pins	H9
RY/BY# (1)	Output	Flash ready busy pin. Will be asserted when write or erase operation completed.	C4

F - RP#	Input	Flash pin which resets the Flash memory. Should be connected to C-RP# on the board	D4
C - RP#	Input	Flash pin which resets the Flash memory. Should be connected to F-RP# on the board	D8
WP#	Input	Flash pin which should be tied to VCC or GND on the board	E3
A0	Input	Address input to Flash memory.	H6
A1	Input	Address input to Flash memory.	G9
A2	Input	Address input to Flash memory	G8
A3	Input	Address input to Flash memory	G7
A4	Input	Address input to Flash memory	H5
A5	Input	Address input to Flash memory	H4
A6	Input	Address input to Flash memory	G6
A7	Input	Address input to Flash memory	G5
A8	Input	Address input to Flash memory	B4
A9	Input	Address input to Flash memory	B6
A10	Input	Address input to Flash memory	B5
A11	Input	Address input to Flash memory	A4
A12	Input	Address input to Flash memory	A8
A13	Input	Address input to Flash memory	A7
A14	Input	Address input to Flash memory	A6
A15	Input	Address input to Flash memory.	A5
A16	Input	Address input to Flash memory.	B3
A17	Input	Address input to Flash memory	G4
A18	Input	Address input to Flash memory	G3
A19	Input	Address input to Flash memory	E5
A20	Input	Address input to Flash memory	A3
DQ0	Input/Output	Data bus that interface with Flash memory and controller	F9
DQ1	Input/Output	Data bus that interface with Flash memory and controller	F10
DQ2	Input/Output	Data bus that interface with Flash memory and controller	E9
DQ3	Input/Output	Data bus that interface with Flash memory and controller	E10
DQ4	Input/Output	Data bus that interface with Flash memory and controller	C9
DQ5	Input/Output	Data bus that interface with Flash memory and controller	C10
DQ6	Input/Output	Data bus that interface with Flash memory and controller	C8
DQ7	Input/Output	Data bus that interface with Flash memory and controller	B10
DQ8	Input/Output	Data bus that interface with Flash memory and controller	F8

DQ9	Input/Output	Data bus that interface with Flash memory and controller	F7
DQ10	Input/Output	Data bus that interface with Flash memory and controller	E8
DQ11	Input/Output	Data bus that interface with Flash memory and controller	E6
DQ12	Input/Output	Data bus that interface with Flash memory and controller	D7
DQ13	Input/Output	Data bus that interface with Flash memory and controller	C7
DQ14	Input/Output	Data bus that interface with Flash memory and controller	B9
DQ15	Input/Output	Data bus that interface with Flash memory and controller	B7