Table 1 shows the I/O pins for the EPC4 100-pin PQFP package.

Table 1. EPC4 Configuration Device Pins			
Pin Name	**Pin Type**	**Description**	**100-Pin PQFP**
EXCLK	Input	External clock source.	61
DCLK	Output	Configuration devices drive this signal to the programmable logic device (PLD) as a configuration clock.	11
DATA0	Output	PLD configuration output data bus.	73
DATA1	Output	PLD configuration output data bus.	84
DATA2	Output	PLD configuration output data bus.	88
DATA3	Output	PLD configuration output data bus.	91
DATA4	Output	PLD configuration output data bus.	96
DATA5	Output	PLD configuration output data bus.	10
DATA6	Output	PLD configuration output data bus.	9
DATA7	Output	PLD configuration output data bus.	8
OE	Open-Drain Input/Output	Configuration devices sense that OE goes high, before starting PLD configuration.	23
nINIT _ CONF	Output	Initiate configuration.	16
nCS	Input	Connected to CONF DONE in the PLD. The PLD will drive it low, when OE is asserted.	60
TDI	Input	Joint Test Action Group (JTAG) data input.	42
TDO	Output	JTAG data output.	44
TMS	Input	JTAG mode selection.	48
TCK	Input	JTAG clock.	35
PGM1	Input	Select one of eight pages that contains configuration data.	13
PGM0	Input	Select one of eight pages that contains configuration data.	14
PGM2	Input	Select one of eight pages that contains configuration data.	15
PORSEL	Input	Select 2 ms or 100 ms power-on reset (POR).	66
TM0	Input	Select test mode for configuration device.	71
TM1	Input	Select test mode for configuration device.	40
GND	Supply	Ground pins.	2, 41, 58, 70, 69, 79
NC	No Connect	No Connect pins.	3, 4,18, 19, 20, 30, 63, 64, 76, 77
Floating (1)	Unconnect	Unconnected pins.	7, 24, 57, 74
BYTE# (2)	Input	Flash byte enable. Connected to VCC.	5
VCC	Supply	Power supply pins.	12, 22, 59, 67, 68, 92
VCCW	Supply	Flash program/erase power supply.	43
C-WE#	Input	Controller write enable pin. Should be connected to F-WE# on the board	33
F-WE#	Input	Flash write enable pin. Should be connected to C-WE# on the board	38
CE#	Input	Flash pin that activates the flash memory.	78
OE#	Input	Flash pin that enables the drivers of the flash output pins.	80
RY/BY# (3)	Output	Flash ready busy pin. Will be asserted when write or erase operation is completed.	37
F-RP#	Input	Flash pin which resets the flash memory. Should be connected to C-RP# on the board.	39
C-RP#	Input	Flash pin which resets the flash memory. Should be connected to F-RP# on the board.	72
WP#	Input	Flash pin which should be tied to VCC or GND on the board.	45
F-A0	Input	Address input to Flash memory. Should be connected to C-A0 on the board.	75
C-A0	Input	Address input to flash memory. Should be connected to F-A0 on the board.	65
F-A1	Input	Address input to flash memory. Should be connected to C-A1 on the board.	56
C-A1	Input	Address input to flash memory. Should be connected to F-A1 on the board.	62
A2	Input	Address input to flash memory.	55
A3	Input	Address input to flash memory.	54
A4	Input	Address input to flash memory.	53
A5	Input	Address input to flash memory.	52
A6	Input	Address input to flash memory.	51
A7	Input	Address input to flash memory.	50
A8	Input	Address input to flash memory.	34
A9	Input	Address input to flash memory.	32
A10	Input	Address input to flash memory.	31
A11	Input	Address input to flash memory.	29
A12	Input	Address input to flash memory.	28
A13	Input	Address input to flash memory.	27
A14	Input	Address input to flash memory.	26
F-A15	Input	Address input to flash memory. Should be connected to C-A15 on the board.	25
C-A15	Input	Address input to flash memory. Should be connected to F-A15 on the board.	21
F-A16	Input	Address input to flash memory. Should be connected to C-A16 on the board.	6
C-A16	Input	Address input to flash memory. Should be connected to F-A16 on the board.	17
A17	Input	Address input to flash memory.	49
A18 (3)	Input	Address input to flash memory.	47
A19 (3)	Input	Address input to flash memory.	46
A20 (3)	Input	Address input to flash memory.	36
DQ0	Input/Output	Data bus that interfaces with flash memory and the controller.	81
DQ1	Input/Output	Data bus that interfaces with flash memory and the controller.	83
DQ2	Input/Output	Data bus that interfaces with flash memory and the controller.	86
DQ3	Input/Output	Data bus that interfaces with flash memory and the controller.	89
DQ4	Input/Output	Data bus that interfaces with flash memory and the controller.	93

Table 1. EPC4 Configuration Device Pins			
Pin Name	**Pin Type**	**Description**	**100-Pin PQFP**
DQ5	Input/Output	Data bus that interfaces with flash memory and the controller.	95
DQ6	Input/Output	Data bus that interfaces with flash memory and the controller.	98
DQ7	Input/Output	Data bus that interfaces with flash memory and the controller.	100
DQ8	Input/Output	Data bus that interfaces with flash memory and the controller.	82
DQ9	Input/Output	Data bus that interfaces with flash memory and the controller.	85
DQ10	Input/Output	Data bus that interfaces with flash memory and the controller.	87
DQ11	Input/Output	Data bus that interfaces with flash memory and the controller.	90
DQ12	Input/Output	Data bus that interfaces with flash memory and the controller.	94
DQ13	Input/Output	Data bus that interfaces with flash memory and the controller.	97
DQ14	Input/Output	Data bus that interfaces with flash memory and the controller.	99
DQ15	Input/Output	Data bus that interfaces with flash memory and the controller.	1

Notes:

(1) These pins are internally connected within the package. Therfore, they should be left unconnected.

(2) BYTE# should be connected to VCC.

(3) A18, A19, and A20 (pins 47, 46, and 36) and RY/BY# (pin 37) should be floating in the EPC4 device.