Pin Name	84-Pin PLCC	144-Pin TQFP	208-Pin PQFP/RQFP
MSEL0 (2)	31	77	108
MSEL1 (2)	32	76	107
nSTATUS (2)	55	35	52
nCONFIG (2)	34	74	105
DCLK (2)	13	107	155
CONF_DONE (2)	76	2	2
INIT_DONE (3)	69	14	19
nCE (2)	14	106	154
nCEO (2)	75	3	3
nWS (4)	80	142	206
nRS (4)	81	141	204
nCS (4)	78	144	208
CS (4)	79	143	207
RDYnBSY (4)	70	11	16
CLKUSR (4)	73	7	10
DATA7 (4)	5	116	166
DATA6 (4)	6	114	164
DATA5 (4)	7	113	162
DATA4 (4)	8	112	161
DATA3 (4)	9	111	159
DATA2 (4)	10	110	158
DATA1 (4)	11	109	157
DATA0 (2), (5)	12	108	156
TDI (2)	15	105	153
TDO (2)	74	4	4
TCK (2)	77	1	1
TMS (2)	57	34	50
TRST (2)	56	(6)	51
Dedicated Inputs	2, 42, 44, 84	54, 56, 124, 126	78, 80, 182, 184
Dedicated Clock Pins	1, 43	55, 125	79, 183
DEV_CLRn (3)	3	122	180
DEV_OE (3)	83	128	186
VCCINT	4, 20, 33, 40, 45, 63	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181
VCCIO	–	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194
GNDINT	26, 41, 46, 68, 82	16, 57, 58, 84, 103, 127	21, 33, 49, 81, 82, 123, 129, 151, 185
GNDIO	–	15, 40, 50, 66, 85, 104, 129, 139	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201
No Connect (N.C.) (7)	–	–	7, 8, 9, 14, 15, 36, 37, 113, 114, 125, 126, 139, 140
Total User I/O Pins (8)	59	102	134

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.