Pin Name	240-Pin PQFP/RQFP	356-Pin BGA	484-Pin FineLine BGA	600-Pin BGA
MSEL0 (2)	124	D4	U4	F5
MSEL1 (2)	123	D3	V4	C1
nSTATUS (2)	60	D24	W19	D32
nCONFIG (2)	121	D2	T7	D4
DCLK (2)	179	AC5	E5	AP1
CONF_DONE (2)	2	AC24	F18	AM32
INIT_DONE (3)	26	T24	K19	AE32
nCE (2)	178	AC2	E4	AN2
nCEO (2)	3	AC22	E19	AP35
nWS (4)	238	AE24	E17	AR29
nRS (4)	236	AE23	F17	AM28
nCS (4)	240	AD24	D19	AL29
CS (4)	239	AD23	D18	AN29
RDYnBSY (4)	23	U22	K17	AG35
CLKUSR (4)	11	AA24	G18	AM34
DATA7 (4)	190	AF4	E8	AM13
DATA6 (4)	188	AD8	G7	AR12
DATA5 (4)	186	AE5	D7	AN12
DATA4 (4)	185	AD6	E7	AP11
DATA3 (4)	183	AF2	F6	AM11
DATA2 (4)	182	AD5	D5	AR10
DATA1 (4)	181	AD4	E6	AN10
DATA0 (2), (5)	180	AD3	D4	AM4
TDI (2)	177	AC3	F5	AN1
TDO (2)	4	AC23	F19	AN34
TCK (2)	1	AD25	E18	AL31
TMS (2)	58	D22	U18	C35
TRST (2)	59	D23	V19	C34
Dedicated Inputs	90, 92, 210, 212	A13, B14, AF14, AE13	E12, H11, R12, V11	C18, D18, AM18, AN18
Dedicated Clock Pins	91, 211	A14, AF13	D12, P11	AL18, E18
DEV_CLRn (3)	209	AD13	G11	AR17
DEV_OE (3)	213	AE14	F12	AR19
VCCINT	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P12, P15, R14, V5, W21, Y8, AA12	A11, A19, B1, B18, D24, E2, F31, F35, H1, K32, M2, N34, P5, T35, U3, V32, Y2, AA33, AB5, AD35, AE4, AF32, AG5, AK31, AK35, AL3, AP24, AR11, AR18
VCCIO	(16)	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13	A20, A27, C2, C3, C4, C8, C15, C23, C32, C33, D5, D31, E5, E12, E31, AL5, AL12, AM5, AM19, AM26, AM31, AN3, AN4, AN8, AN15, AN32, AN33, AP34, AR23
VCC_CKLK (14)	–	–	–	–

Pin Name	240-Pin PQFP/RQFP	356-Pin BGA	484-Pin FineLine BGA	600-Pin BGA
GNDINT	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W11, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16	A1, A2, A3, A4, A5, A18, A31, A32, A33, A34, A35, B2, B3, B4, B5, B6, B31, B32, B33, B34, B35, C5, C6, C30, C31, D6, D30, E6, AN35
GNDIO	–	–	–	E30, AL6, AL30, AM6, AM30, AN5, AN6, AN30, AN31, AP2, AP3, AP4, AP5, AP6, AP30, AP31, AP32, AP33, AR1, AR2, AR3, AR4, AR5, AR30, AR31, AR32, AR33, AR34, AR35
GND_CKLK (14)	–	–	–	–
No Connect (N.C.)	–	–	–	D1, D2, D3, E1, E3, E4, E32, F1, F2, F3, F4, G1, G2, G3, G4, G5, H5, D33, D34, D35, E33, E34, E35, F32, F33, F34, G31, G32, G33, G34, G35, H31, AB31, AB32, AB33, AB34, AC31, AC32, AC33, AC34, AC35, AD31, AD32, AD33, AD34, AE33, AE34, AE35, AH5, AJ2, AJ3, AJ4, AJ5, AK1, AK2, AK3, AK4, AK5, AL1, AL2, AL4, AM1, AM2, AM3 (15)
Total User I/O Pins (8)	189	274	369	406

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.