Pin Name	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP/RQFP	256-Pin FineLine BGA
MSEL0 (2)	54	77	108	P1
MSEL1 (2)	53	76	107	R1
nSTATUS (2)	25	35	52	T16
nCONFIG (2)	51	74	105	N4
DCLK (2)	75	107	155	B2
CONF_DONE (2)	1	2	2	C15
INIT_DONE (3)	10	14	19	G16
nCE (2)	74	106	154	B1
nCEO (2)	2	3	3	B16
nWS (4)	97	142	206	B14
nRS (4)	96	141	204	C14
nCS (4)	99	144	208	A16
CS (4)	98	143	207	A15
RDYnBSY (4)	8	11	16	G14
CLKUSR (4)	5	7	10	D15
DATA7 (4)	84	116	166	B5
DATA6 (4)	82	114	164	D4
DATA5 (4)	81	113	162	A4
DATA4 (4)	80	112	161	B4
DATA3 (4)	79	111	159	C3
DATA2 (4)	78	110	158	A2
DATA1 (4)	77	109	157	B3
DATA0 (2), (5)	76	108	156	A1
TDI (2)	73	105	153	C2
TDO (2)	3	4	4	C16
TCK (2)	100	1	1	B15
TMS (2)	24	34	50	P15
TRST (2)	(6)	(6)	51	R16
Dedicated Inputs	40, 38, 89, 91	54, 56, 124, 126	78, 80, 182, 184	B9, E8, M9, R8
Dedicated Clock Pins	39, 90	55, 125	79, 183	A9, L8
DEV_CLRn (3)	87	122	180	D8
DEV_OE (3)	93	128	186	C9
VCCINT	18, 37, 52, 66, 88	6, 25, 52, 53, 75, 93, 123	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L9, L12, M11, R2
VCCIO	4, 17, 32, 49, 67, 83	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12
GNDINT	12, 41, 59, 92	16, 57, 58, 84, 103, 127	21, 33, 49, 81, 82, 123, 129, 151, 185	E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K7,K10, L6, L11, M5, M12, T8
GNDIO	11, 28, 46, 60, 72, 95	15, 40, 50, 66, 85, 104, 129, 139	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–

Pin Name	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP/RQFP	256-Pin FineLine BGA
No Connect (N.C.) (7)	–	–	7, 8, 9, 14, 15, 36, 37, 113, 114, 125, 126, 139, 140	A8, B8, D1, D14, D16, E1, E3, E13, E14, E15, E16, F14, F15, F16, G3, H1, H4, H16, J1, J2, K2, K3, K12, K14, K15, K16, L2, L4, M2, M3, M4, M14, M16, N1, N2, N3, N14, N15, P2, P11, P14 (7)
Total User I/O Pins (8)	66	102	134	150

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.