Pin Name	599-Pin PGA	600-Pin BGA
MSEL0 (2)	F6	F5
MSEL1 (2)	C3	C1
nSTATUS (2)	E43	D32
nCONFIG (2)	B4	D4
DCLK (2)	BE5	AP1
CONF_DONE (2)	BC43	AM32
INIT_DONE (3)	AM40	AE32
nCE (2)	BB6	AN2
nCEO (2)	BF44	AP35
nWS (4)	BB40	AR29
nRS (4)	BA37	AM28
nCS (4)	AY38	AL29
CS (4)	BA39	AN29
RDYnBSY (4)	AW47	AG35
CLKUSR (4)	AY42	AM34
DATA7 (4)	BD14	AM13
DATA6 (4)	BA17	AR12
DATA5 (4)	BB16	AN12
DATA4 (4)	BF12	AP11
DATA3 (4)	BG11	AM11
DATA2 (4)	BG9	AR10
DATA1 (4)	BF10	AN10
DATA0 (2), (5)	BC5	AM4
TDI (2)	BF4	AN1
TDO (2)	BB42	AN34
TCK (2)	BE43	AL31
TMS (2)	F42	C35
TRST (2)	B46	C34
Dedicated Inputs	B24, C25, BG25, BG23	C18, D18, AM18, AN18
Dedicated Clock Pins	BF24, A25	AL18, E18
LOCK (12)	–	–
GCLK1 (13)	–	–
DEV_CLRn (3)	BE23	AR17
DEV_OE (3)	BC25	AR19
VCCINT	A3, A45, C1, C11, C19, C29, C37, C47, E5, G25, L3, L45, W3, W45, AJ3, AJ45, AU3, AU45, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45	A11, A19, B1, B18, D24, E2, F31, F35, H1, K32, M2, N34, P5, T35, U3, V32, Y2, AA33, AB5, AD35, AE4, AF32, AG5, AK31, AK35, AL3, AP24, AR11, AR18
VCCIO	D24, E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AD4, AD44, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27,	A20, A27, C2, C3, C4, C8, C15, C23, C32, C33, D5, D31, E5, E12, E31, AL5, AL12, AM5, AM19, AM26, AM31, AN3, AN4, AN8, AN15, AN32, AN33, AP34, AR23
VCC_CKLK (14)	–	–
GNDINT	A47, B2, C13, C21, C27, C35, C45, D4, G23, N3, N45, AA3, AA45, AG3, AG45, AR3, AR45, BD44, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47	A1, A2, A3, A4, A5, A18, A31, A32, A33, A34, A35, B2, B3, B4, B5, B6, B31, B32, B33, B34, B35, C5, C6, C30, C31, D6, D30, E6, AN35

Pin Name	599-Pin PGA	600-Pin BGA
GNDIO	E7, E13, E19, E29, E35, E41, F24, G5, G43, H40, N5, N43, W5, W43, AD6, AD42, AJ5, AJ43, AR5, AR43, AY8, AY40, BA5, BA43, BB24, BC7, BC13, BC19, BC29, BC35,	E30, AL6, AL30, AM6, AM30, AN5, AN6, AN30, AN31, AP2, AP3, AP4, AP5, AP6, AP30, AP31, AP32, AP33, AR1, AR2, AR3, AR4, AR5, AR30, AR31, AR32, AR33, AR34, AR35
GND_CKLK (14)	–	–
No Connect (N.C.)	–	–
Total User I/O Pins (8)	470	470

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.