Pin Name	208-Pin PQFP/RQFP	240-Pin PQFP/RQFP	356-Pin BGA
MSEL0 (2)	108	124	D4
MSEL1 (2)	107	123	D3
nSTATUS (2)	52	60	D24
nCONFIG (2)	105	121	D2
DCLK (2)	155	179	AC5
CONF_DONE (2)	2	2	AC24
INIT_DONE (3)	19	26	T24
nCE (2)	154	178	AC2
nCEO (2)	3	3	AC22
nWS (4)	206	238	AE24
nRS (4)	204	236	AE23
nCS (4)	208	240	AD24
CS (4)	207	239	AD23
RDYnBSY (4)	16	23	U22
CLKUSR (4)	10	11	AA24
DATA7 (4)	166	190	AF4
DATA6 (4)	164	188	AD8
DATA5 (4)	162	186	AE5
DATA4 (4)	161	185	AD6
DATA3 (4)	159	183	AF2
DATA2 (4)	158	182	AD5
DATA1 (4)	157	181	AD4
DATA0 (2), (5)	156	180	AD3
TDI (2)	153	177	AC3
TDO (2)	4	4	AC23
TCK (2)	1	1	AD25
TMS (2)	50	58	D22
TRST (2)	51	59	D23
Dedicated Inputs	78, 80, 182, 184	90, 92, 210, 212	A13, B14, AF14, AE13,
Dedicated Clock Pins	79, 183	91, 211	A14, AF13
DEV_CLRn (3)	180	209	AD13
DEV_OE (3)	186	213	AE14
VCCINT	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224	A1, A26, C14, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26
VCCIO	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	(16)	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16
GNDINT	21, 33, 49, 81, 82, 123, 129, 151, 185	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	A2, A10, A20, B1, B13, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19,
GNDIO	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–	–

Pin Name	208-Pin PQFP/RQFP	240-Pin PQFP/RQFP	356-Pin BGA
No Connect (N.C.) (7)	–	–	C1, D1, D26, E1, E2, G1, G5, G23, G26, H1, H25, H26, J25, K25, P24, R24, T23, U25, V1, V3, V4, V26, W2, W3, Y1, Y2, Y23, AC26 (9)
Total User I/O Pins (8)	147	189	246

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.