Pin Name	208-Pin PQFP/RQFP	240-Pin PQFP/RQFP
MSEL0 (2)	108	124
MSEL1 (2)	107	123
nSTATUS (2)	52	60
nCONFIG (2)	105	121
DCLK (2)	155	179
CONF_DONE (2)	2	2
INIT_DONE (3)	19	26
nCE (2)	154	178
nCEO (2)	3	3
nWS (4)	206	238
nRS (4)	204	236
nCS (4)	208	240
CS (4)	207	239
RDYnBSY (4)	16	23
CLKUSR (4)	10	11
DATA7 (4)	166	190
DATA6 (4)	164	188
DATA5 (4)	162	186
DATA4 (4)	161	185
DATA3 (4)	159	183
DATA2 (4)	158	182
DATA1 (4)	157	181
DATA0 (2), (5)	156	180
TDI (2)	153	177
TDO (2)	4	4
TCK (2)	1	1
TMS (2)	50	58
TRST (2)	51	59
Dedicated Inputs	78, 80, 182, 184	90, 92, 210, 212
Dedicated Clock Pins	79, 183	91, 211
DEV_CLRn (3)	180	209
DEV_OE (3)	186	213
VCCINT	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181	5, 16, 27, 37, 47, 57, 77, 89, 96, 112, 122, 130, 140, 150, 160, 170, 189, 205, 224
VCCIO	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	(16)
GNDINT	21, 33, 49, 81, 82, 123, 129, 151, 185	10, 22, 32, 42, 52, 69, 85, 93, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232
GNDIO	20, 32, 48, 59, 72, 91, 124, 130, 152, 171, 188, 201	–
No Connect (N.C.) (7)	–	–
Total User I/O Pins (8)	147	189

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.