Pin Name (1)	144-Pin TQFP EPF6024A	208-Pin PQFP EPF6024A	240-Pin PQFP EPF6024A	256-Pin BGA EPF6024A	256-Pin FineLine BGA EPF6024A
MSEL (2)	33	46	52	T3	L5
nSTATUS (2)	56	80	92	W11	K8
nCONFIG (2)	53	77	89	Y11	N8
DCLK (2)	128	184	212	C10	G9
CONF_DONE (2)	105	150	172	E18	F12
INIT_DONE (3)	94	135	155	J19	H13
nCE (2)	4	6	9	E1	F5
nCEO (4)	70	102	117	V18	N12
nWS (4)	117	169	195	B15	F10
nRS (4)	120	174	200	C13	D10
nCS (4)	111	159	184	B17	D12
CS (4)	114	162	188	A17	F11
RDYnBUSY (4)	97	140	161	G20	G13
CLKUSR	100 (4)	144	166	G17	F13
DATA (2), (5)	125	181	209	B10	D9
TDI (6)	13	19	22	J3	G5
TDO (6)	73	107	124	T17	N13
TCK	34 (6), (7)	47	54	V1	K6
TMS	27 (6)	38	44	P3	K5
Dedicated Inputs	17, 20, 89, 92	24, 28, 128, 132	28, 32, 148, 152	K19, L1, L3, L20	H4, H5, J12, J13
DEV_CLRn (3)	130	187	216	C9	E8
DEV_OE (3)	123	178	205	A12	E9
VCCINT	6, 31, 77, 103	8, 26, 44, 111, 130, 148	11, 30, 50, 130, 150, 170	D20, F3, K20, L2, T20, U1	G10, H7, H8, J9, J10, K7
VCCIO	7, 19, 32, 55, 78, 91, 104, 127	9, 27, 45, 63, 79, 96, 112, 131, 149, 166, 183, 200	12, 31, 51, 72, 91, 110, 131, 151, 171, 192, 211, 230	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	B5, B8, C13, C16, E2, G1, J16, N16, P1, P12, R4, R8
GND	5, 18, 30, 54, 76, 90, 102, 126	7, 25, 43, 62, 78, 95, 110, 129, 147, 165, 182, 199	10, 29, 49, 61, 71, 90, 109, 120, 129, 149, 169, 181, 191, 210, 229, 240	A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13, U17	A1, A16, B2, B15, G7, H9, H10, J7, J8, K10, P3, R15, T16
No connect (N.C.)	–	–	–	–	–
Total user I/O pins (8)	117	171	199	218	219

Notes:
(1) All pins not listed are user I/O pins.
(2) This pin is a dedicated configuration or JTAG pin; therefore, it is not available for use as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its chip-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin. If the JTAG BST circuitry device option is not used, JTAG testing may still be performed before configuration.
(7) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(8) The user I/O count includes dedicated input and I/O pins.