

Dedicated Pin	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP
INPUT/GCLK1	83	87	89	139
INPUT/GCLRn	1	89	91	141
INPUT/OE1	84	88	90	140
INPUT/OE2/GCLK2	2	90	92	142
TDI (4)	14	4	6	9
TMS (4)	23	15	17	22
TCK (4)	62	62	64	99
TDO (4)	71	73	75	112
GND	7, 19, 32, 42, 47, 59, 72, 82	38, 86, 11, 26, 43, 59, 74, 95	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCCINT (5.0 V only)	3, 43	39, 91	41, 93	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82	5, 20, 36, 53, 68, 84	8, 26, 55, 79, 104, 133
No Connect (N.C.)	6, 39, 46, 79	—	—	1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O Pins (5)	60	80	80	100

LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP
A	1	11	100	2	158
A	2	—	—	—	—
A	3	10	99	1	153
A	4	—	—	—	—
A	5	—	—	—	152
A	6	—	98	100	151
A	7	—	—	—	—
A	8	9	97	99	150
A	9	8	96	98	149
A	10	—	—	—	—
A	11	5	94	96	147
A	12	—	—	—	—
A	13	—	—	—	146
A	14	—	93	95	145
A	15	—	—	—	—
A	16	4	92	94	144
B	17	18	9	11	15
B	18	—	—	—	—
B	19	17	8	10	14
B	20	—	—	—	—
B	21	—	—	—	13
B	22	—	7	9	12
B	23	—	—	—	—
B	24	16	6	8	11
B	25	15	5	7	10
B	26	—	—	—	—
B	27	14 (4)	4 (4)	6 (4)	9 (4)
B	28	—	—	—	—
B	29	—	—	—	7
B	30	—	2	4	160
B	31	—	—	—	—
B	32	12	1	3	159
C	33	—	19	21	27
C	34	—	—	—	—
C	35	25	17	19	25
C	36	—	—	—	—
C	37	—	—	—	24
C	38	24	16	18	23
C	39	—	—	—	—
C	40	23 (4)	15 (4)	17 (4)	22 (4)
C	41	—	10	12	16
C	42	—	—	—	—
C	43	20	12	14	18
C	44	—	—	—	—
C	45	—	—	—	19
C	46	21	13	15	20
C	47	—	—	—	—
C	48	22	14	16	21

LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP
D	49	—	—	—	48
D	50	—	—	—	—
D	51	33	28	30	44
D	52	—	—	—	—
D	53	—	27	29	43
D	54	31	25	27	41
D	55	—	—	—	—
D	56	30	24	26	33
D	57	—	—	—	32
D	58	—	—	—	—
D	59	29	23	25	31
D	60	—	—	—	—
D	61	—	22	24	30
D	62	28	21	23	29
D	63	—	—	—	—
D	64	27	20	22	28
E	65	—	—	—	59
E	66	—	—	—	—
E	67	41	37	39	58
E	68	—	—	—	—
E	69	—	36	38	57
E	70	40	35	37	56
E	71	—	—	—	—
E	72	37	33	35	54
E	73	—	—	—	53
E	74	—	—	—	—
E	75	36	32	34	52
E	76	—	—	—	—
E	77	—	31	33	51
E	78	35	30	32	50
E	79	—	—	—	—
E	80	34	29	31	49
F	81	—	—	—	62
F	82	—	—	—	—
F	83	44	40	42	63
F	84	—	—	—	—
F	85	—	41	43	64
F	86	45	42	44	65
F	87	—	—	—	—
F	88	48	44	46	67
F	89	—	—	—	68
F	90	—	—	—	—
F	91	49	45	47	69
F	92	—	—	—	—
F	93	—	46	48	70
F	94	50	47	49	71
F	95	—	—	—	—
F	96	51	48	50	72

LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP
G	97	—	—	—	73
G	98	—	—	—	—
G	99	52	49	51	77
G	100	—	—	—	—
G	101	—	50	52	78
G	102	54	52	54	80
G	103	—	—	—	—
G	104	55	53	55	88
G	105	—	—	—	89
G	106	—	—	—	—
G	107	56	54	56	90
G	108	—	—	—	—
G	109	—	55	57	91
G	110	57	56	58	92
G	111	—	—	—	—
G	112	58	57	59	93
H	113	—	58	60	94
H	114	—	—	—	—
H	115	60	60	62	96
H	116	—	—	—	—
H	117	—	—	—	97
H	118	61	61	63	98
H	119	—	—	—	—
H	120	62 (4)	62 (4)	64 (4)	99 (4)
H	121	—	67	69	105
H	122	—	—	—	—
H	123	65	65	67	103
H	124	—	—	—	—
H	125	—	—	—	102
H	126	64	64	66	101
H	127	—	—	—	—
H	128	63	63	65	100
I	129	67	68	70	106
I	130	—	—	—	—
I	131	68	69	71	107
I	132	—	—	—	—
I	133	—	—	—	108
I	134	—	70	72	109
I	135	—	—	—	—
I	136	69	71	73	110
I	137	70	72	74	111
I	138	—	—	—	—
I	139	71 (4)	73 (4)	75 (4)	112 (4)
I	140	—	—	—	—
I	141	—	—	—	114
I	142	—	75	77	121
I	143	—	—	—	—
I	144	73	76	78	122

LAB	MC	84-Pin PLCC	100-Pin TQFP (1), (2)	100-Pin PQFP (3)	160-Pin PQFP
J	145	74	77	79	123
J	146	—	—	—	—
J	147	75	78	80	128
J	148	—	—	—	—
J	149	—	—	—	129
J	150	—	79	81	130
J	151	—	—	—	—
J	152	76	80	82	131
J	153	77	81	83	132
J	154	—	—	—	—
J	155	80	83	85	134
J	156	—	—	—	—
J	157	—	—	—	135
J	158	—	84	86	136
J	159	—	—	—	—
J	160	81	85	87	137

Notes:

- (1) EPM7160E devices are not available in the 100-pin TQFP package.
- (2) A complete thermal analysis should be performed before committing a design to this device package.
- (3) EPM7160S devices are not available in the 100-pin PQFP package.
- (4) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for BST or with ISP, this pin is not available as a user I/O pin.
- (5) The user I/O pin count includes dedicated input pins and all I/O pins.

Copyright © 1995, 1996, 1997, 1998, 1999, 2000, 2001 Altera Corporation,
101 Innovation Drive, San Jose, CA 95134, USA, all rights reserved.

By accessing this information, you agree to be bound by the terms of Altera's Legal Notice.