Utilizing the Burst Mode Flash in a Motorola MPC555 System

Application Note

Burst mode devices offer improvements in system speed and performance by reducing sequential read access times. AMD’s Am29BL162 and Am29BL802 devices offer a cost-effective, low-power, high performance solution with a synchronous burst interface that “gluelessly” interfaces to Motorola’s MPC555 controller. Taking advantage of the burst read capability, AMD’s devices offer an average access time reduction of more than 65 percent for an eight-word sequential read at 40 MHz. In the normal asynchronous mode, the read access time is as fast as 65 ns per byte. For a burst mode operation, the initial access time is as fast as 65 ns followed by sequential byte transfers of 18 ns each.

This document shows how to implement AMD’s burst mode devices to the MPC555 processor.

BACKGROUND

Motorola MPC555

Motorola has developed a powerful 32-bit, PowerPC based microcontroller (MPC555) primarily targeted for high performance automotive applications. The MPC555 was designed to operate over an extended temperature range of –40°C to +125°C, on a 3.3-volt power supply, operating at frequencies up to 40 MHz.

Burst Mode Flash

The Am29BL162 and Am29BL802 are high performance 16 Mbit and 8 Mbit single power supply 3.0 Volt-only Flash memory devices. The Am29BL162 is organized as 1 Mbyte of 16 bits each, and the Am29BL802 is organized as 0.5 Mbyte of 16 bits each. These devices are designed to be programmed in-system with the standard system 3.3-volt \( V_{CC} \) supply. Neither a 12.0-volt or 5.0-volt \( V_{PP} \) is required for program or erase operations. The Am29BL162 and Am29BL802 provide truly high performance, non-volatile Flash memory solution. At an industrial temperature range (–40°C to 85°C) and a \( V_{CC} \) of 3.0–3.6 V, the Am29BL162 and Am29BL802 devices provide burst accesses as fast as 17 ns with an initial access times of 65 ns. At an extended temperature range (–55°C to 125°C) and a \( V_{CC} \) of 3.3 V ± 5%, the Am29BL162 and Am29BL802 devices provide burst access as fast as 18 ns with initial access times of 65 ns.

IMPLEMENTATION

The connections between the MPC555 and AMD’s Burst mode devices can be seen in Figure 1 and Figure 2. The MPC555 processor and the Flash device can be implemented without the use of additional logic. Descriptions of the interface connections are discussed below:

Address and Data Bus Connections

The MPC555 address and data buses connect to the corresponding address and data buses of the Flash. The address bus connections give the processor a medium for specifying which word is to be accessed. The address lines of the MPC555 processor are referenced as bits 31–0 with bit 32 being the least significant bit. Therefore, bits 31–12 of the MPC555 must be connected to address lines A0–A19 of the Flash.

The data bus pin connections provide a pathway for data to be transferred. Data pins 0–15 of the MPC555 connect in a bit reversed order to the DQ15–DQ0 pins of the Flash device.

MPC555 CSx# to Flash CE#

MPC555 CSx# (output)—The MPC555 provides four separate chip select pins. The CSx# pins are output signals from the MPC555 that enable peripheral devices and external memory. CS0 can be configured to be a global chip select for boot devices.

Flash CE# (input)—The Flash chip enable CE# pin is driven high only when the Flash device is set to standby mode or when the burst read cycle is terminated. Otherwise, the signal is set low during read/program operations.

Connection—The MPC555 processor provides chip select timing mechanisms allowing it to be implemented gluelessly with several types of memory devices. When the MPC555 drives the Chip Select signal low, the Flash is activated.
MPC555 WEx# to Flash WE#

MPC555 WEx# (output) — When the signal is asserted (low) the device is executing a write instruction. A high indicates the processor is executing to read operation.

Flash WE# (input) — The WE# signal is asserted only for program/erase operations. WE# must be driven high to perform a device read operation, in burst and regular modes.

Connection — The function of RD/WR# from the MPC555 is to be at a logic low level when the processor is doing a data write. When the processor is performing a data read, the RD/WR# signal is logically high.

MPC555 Transfer Start (TS#) to Flash Load Burst Address (LBA#)

MPC555 TS# (output) — The transfer start (TS#) signal indicates the start of a bus cycle. The processor asserts the signal when it gains access to the external bus.

Flash LBA# (input) — The LBA# signal indicates that a valid address is present on the address inputs. When LBA# is low at the rising edge of the clock, the initial address is latched into the Flash device.

Connection — The transfer start (TS#) pin from the MPC555 connects to the LBA# pin of the Flash. At the start of a data read transaction, the processor asserts the TS# pin. Driving TS# low forces LBA# low, loading the address into the Flash at the rising clock edge. This transaction is necessary in both a regular mode read, and burst mode read operations.

MPC555 BDIP# to Flash Burst Address Advance (BAA#)

MPC555 BDIP# (output) — The burst data in progress pin indicates that a burst transaction is taking place. It is asserted at the beginning of the burst cycle and is negated before the last data word transfer. The timing is controlled by the microcontroller.

Flash BAA# (input) — The BAA# pin triggers the auto-increment feature of the memory device. When BAA# is asserted (low) the flash increments the current address to the next sequential address. For a Burst sequence, BAA# is driven low when the first data word is placed on the bus. BAA# is negated when the flash places the second to last data word on the bus.

Connection — The Burst Data in Progress signal (BDIP#) from the MPC555 connects to BAA# of the Flash. The signal is asserted after the first data word of a burst sequence is presented on the bus from the Flash. The signal is negated at the same time the last data word of the burst sequence is put on the bus.

MPC555 OE# to Flash OE#

MPC555 OE# (output) — This output line is asserted when a read access to an external slave controlled by the memory controller is initiated by the MPC555.

Flash OE#: OE# (input) — The output enable (OE#) signal should be driven low by the master when a read operation is initiated.

Connection — OE# from the MPC555 is driven low during a read transaction. The OE# signal from the Flash is asserted when reading data from the Flash device.
MPC555 PROGRAMMING

Operating the MPC555 processor and the Am29BL162 or Am29BL802 without additional logic requires appropriate bit settings of the memory controller option register within the MPC555 processor. The bit fields that must be correctly set are the SETA bit, SCY bit field, and the BSCY bit field.

**SETA Bit**—SETA (external transfer acknowledge bit) must be set to zero. When the SETA bit is set to zero, the memory controller in the MPC555 processor internally generates acknowledgement signals during bus transfers. If this bit is set to one, slave devices must externally provide the acknowledgment signals during the data transmission.

**SCY Bits**—Bits 24–27 make up the SCY field in the memory controller option register. The SCY field denotes the number of wait state that must be inserted during a single word transfer or during the initial transfer of a burst transfer sequence. This field should be programmed to 2 indicating that two wait states are needed during the initial word transfer.

**BSCY Bits**—Bits 28–31 make up the BSCY field in the memory controller option register. The BSCY field denotes the number of wait states that must be inserted during a burst sequence (after the initial access) should be programmed to 00 when using the Am29BLXXX devices.

**LBDIP Bit**—To support different types of memory devices, the MPC supports two types of timing for the BDIP# signal: normal and late. For the Am29BLXXX the late timing should be chosen. To do so set the LBDIP bit in the BR register (LBDIP = 1). This is needed to delay the BDIP# by the number of wait states in the first data beat.
Timing Considerations

To ensure proper data transmission, timing parameters of the MPC555 and the Flash must be obeyed. Formulations for initial access times is illustrated in the following equation:

\[ t_{\text{ACC}} = ((n-1) \times t_{\text{CYCLE}}) - t_{\text{SETI}} - t_{\text{SYSMGN}} \]

where

- \( t_{\text{ACC}} \) = Initial access time
- \( n \) = Number of clock cycles
- \( t_{\text{CYCLE}} \) = Clock period
- \( t_{\text{SETI}} \) = Microcontroller/Microprocessor setup time
- \( t_{\text{SYSMGN}} \) = System design margin time

\( n \) is equal to the number of clock periods. \( n \) is also equal to the number of wait states being inserted plus 1. So, using \( n = 4 \) indicates a calculation is being made for three wait states (i.e. the data is ready on the third clock cycle). \( t_{\text{SYSMGN}} \) and \( t_{\text{SETI}} \) are general values based on common system and microprocessor values. With a system clock frequency of 40 MHz, the values for \( t_{\text{SETI}} \) and \( t_{\text{SYSMGN}} \) are 6 ns and 1 ns respectively. \( t_{\text{ACC}} \) is measured from the second clock of the read access. At 40 Mhz, with three wait states, \( t_{\text{ACC}} \) is calculated to be 68 ns. Therefore, to incorporate three wait states at a clock frequency of 40 MHz the initial access time must be less than 68 ns.

For burst access time calculations the following equation is used.

\[ t_{\text{BACC}} = (n \times t_{\text{CYCLE}}) - t_{\text{SETB}} - t_{\text{SYSMGNB}} \]

where \( t_{\text{BACC}} \) = burst access time

Again, using a system clock frequency of 40 MHz values for \( t_{\text{SETB}} \) and \( t_{\text{SYSMGNB}} \) were determined. \( t_{\text{SETB}} \) and \( t_{\text{SYSMGNB}} \) are 6 ns and 1 ns respectively at a system clock frequency of 40 MHz. Carrying out the calculation for \( t_{\text{BACC}} \) at 40 MHz results to 18 ns. \( t_{\text{BACC}} \) indicates the burst access time must be less than 18 ns to ensure proper functionality.

Based on the above calculations AMD’s Am29BL162 and Am29BL802 devices support the MPC555 processor using 4-1-1-1 timing at a system clock frequency of 40 MHz. 4-1-1-1 timing is equivalent to 3-0-0-0 wait states for a burst data transaction. AMD’s Burst mode devices have an initial access time of 65 ns and a burst access time of 18 ns.

Functional Characteristics

When the host processor performs a fetch to a Burst mode flash device, it places the pre-specified address across the address bus. The processor also drives the appropriate control signals to access the data from the flash device. The initial memory access is measured from the second clock and requires 65 ns delay in order to supply the processor with the correct data. Thus with a system clock of 40 MHz (25 ns clock period), the flash requires that the system assert three wait states in order for valid data to appear on the data bus (initial \( t_{\text{ACC}} \) on the Am29BL162 or Am29BL802 data sheet). AMD’s Burst mode devices are able to communicate with the MPC555 processor without the use of additional logic.
REVISION SUMMARY

Revision B (February 24, 2000)
Figure 2, Circuit Layout (32-Bit Configuration)
Corrected path from data bus of MPC555 processor to data bus of two Am29BL162CB flash devices.

Revision B+1 (January 5, 2001)
MPC555 WEx# to Flash WE#
Corrected typographical errors.

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