NetSC520 Demonstration Board

User's Manual

Order #24323A

AMD

NetSC520 Demonstration Board User’s Manual, order #24323A

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About the NetSC520 Demonstration Board

The AMD NetSC520 demonstration board is a small board combining AMD's Élan™SC520 microcontroller with an AMD Am79C973 PCnet™-*FAST III* 10/100 Mbit/s Ethernet controller, 16 Mbytes of synchronous DRAM (SDRAM), and 16 Mbytes of execute-in-place (XIP) Flash memory. The board demonstrates a simple, low-cost Ethernet capability that can be added to a wide variety of embedded networking applications. See Figure 2-1 on page 2-2 for a block diagram of the demonstration board.

Typical applications of the demonstration board design include low-cost, managed Ethernet hubs, "smart house" components, industrial control, point-of-sale terminals, and software development tools such as ROM emulators. An entire new class of applications known as "net appliances", ranging from electric utility meters to coffee pots, could also use a design similar to that of the NetSC520 demonstration board.

The NetSC520 demonstration board is based upon the ÉlanSC520 microcontroller. The microcontroller provides an industry-standard x86 architecture CPU, integrated with a 33-MHz, 32-bit PCI bus, 8- and 16-bit general-purpose (GP) bus, high-performance SDRAM controller, ROM/Flash controller, integrated peripherals, and a variety of other features including system test and debug functions.

The NetSC520 demonstration board is designed with the PC/104-Plus expansion interface, which provides access to the ÉlanSC520 microcontroller's PCI bus and GP-bus expansion signals.

Demonstration Board Features

The NetSC520 demonstration board provides the following features. For details see “Board Functional Description” on page 2-1.

- ÉlanSC520 microcontroller
- AMD Am79C973 PCnet-*FAST III* single-chip 10/100 Mbit/s Ethernet controller
- 16 Mbytes SDRAM
- 16 Mbytes XIP Flash memory
- Two 1-Kbyte serial EEPROM memories (one for Ethernet configuration, one for general use)
- PC/104-Plus expansion interface (embedded PCI and ISA-compatible interfaces)
- One RJ-45 connector for 10/100Base-T twisted-pair Ethernet connection
- Two RS-232 serial ports with DB-9 connectors
- One 2-mm-pitch IDE interface
- LEDs are provided to indicate power status and the activity of serial, Ethernet, and IDE interfaces. Additional software-controlled LEDs are provided via nine Programmable IO (PIO) signals.
- Eight software-defined bootstrap configuration switches
- Three system-defined bootstrap configuration switches
- 12-V external power supply (AC wall adapter)
- Onboard power supplies for 2.5 V, 3.3 V, and 5 V
- Banana jacks for external supply of PC/104-Plus voltages not provided on-board: –12 V and –5 V
- Battery backup for the microcontroller’s real-time clock (RTC)
- Reset circuitry with onboard reset button and header for external switch
- Port for JTAG and AMDebug™ technology debugging

BIOS, debugging, and utility software is included with the kit. Additional related software and information is published as it becomes available via the Embedded Processors, CodeKits section of **www.amd.com**.

Block Diagram

Figure 0-1 shows a block diagram of the NetSC520 demonstration board.

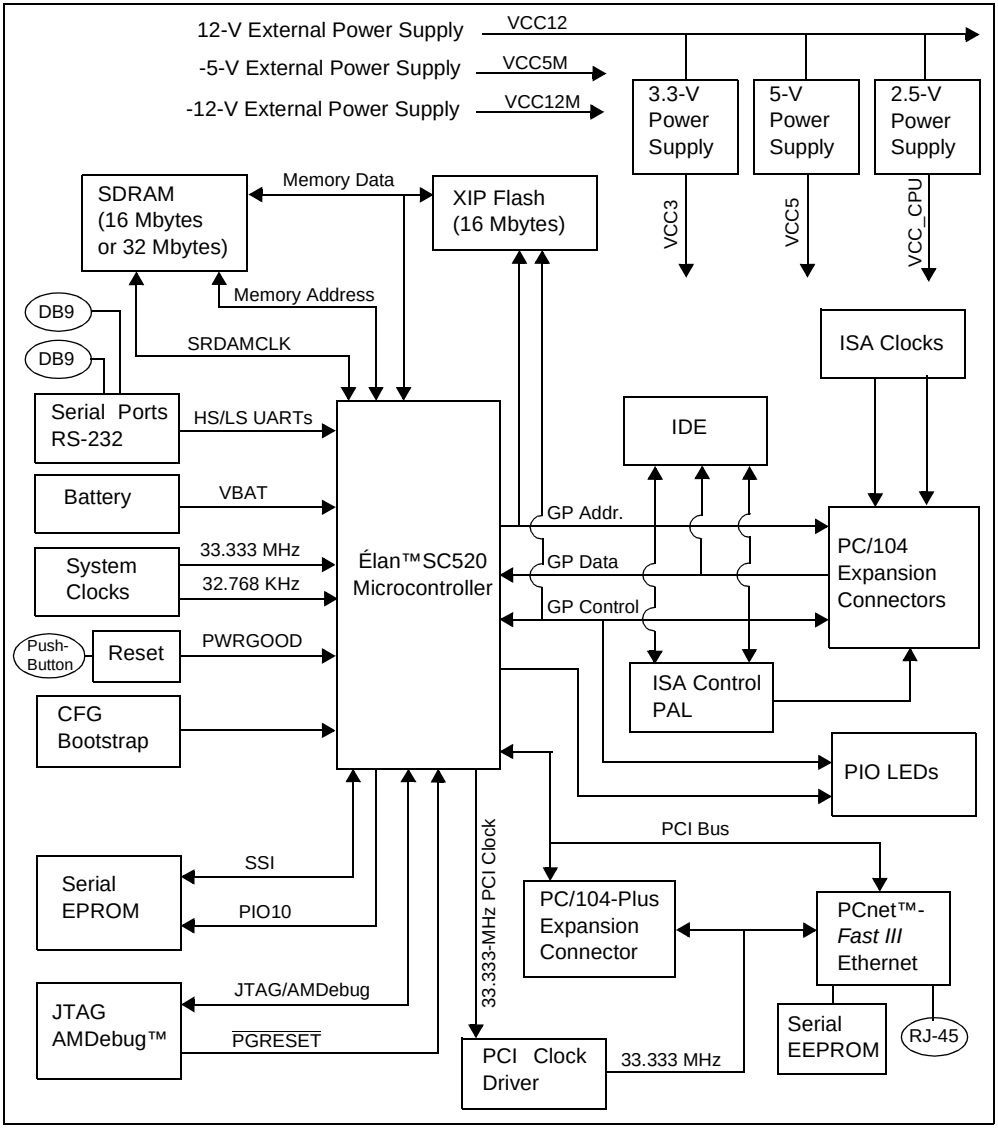


Figure 0-1. NetSC520 Demonstration Board Block Diagram

Documentation

The *NetSC520 Demonstration Board User's Manual* provides information on the design and function of the demonstration board.

About this Manual

Chapter 1, "Quick Start" provides installation and set-up information for the demonstration board.

Chapter 2, "Board Functional Description" contains descriptions of the basic sections of the demonstration board including: microcontroller, memory, interfaces, reset logic, power supply, and any other important features of the board.

Appendix A, "Jumper and Dip Switch Settings" explains how to set up the board's various jumpers and switches.

Appendix B, "Board Routing Rules" provides information useful in laying out designs similar to the NetSC520 demonstration board.

An Index is also included.

Suggested Reference Material

For information on ordering the literature listed below, see "Documentation and Literature Support" on page iii.

- *Élan™SC520 Microcontroller Data Sheet*
  Advanced Micro Devices, order #22003
- *Élan™SC520 Microcontroller User's Manual*
  Advanced Micro Devices, order #22004
- *Élan™SC520 Microcontroller Register Set Manual*
  Advanced Micro Devices, order #22005
- *Am79C973/Am79C975 PCnet™*-FAST III *Single-Chip 10/100 Mbps PCI Ethernet Controller with Integrated PHY Data Sheet*
  Advanced Micro Devices, order #21510

For current application notes, technical bulletins, and CodeKit software, see **www.amd.com**.

Chapter 1

Quick Start

This chapter provides information that helps you quickly set up and start the NetSC520 demonstration board.

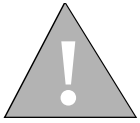
The NetSC520 demonstration board can be controlled using AMDebug™ technology, independently of any software installed on the board, via a JTAG-compatible debugging interface such as the Macraigor Systems LLC Raven-AMD device. The Raven device provides typical monitor/debugger functionality on an attached PC running the REMON software included with your kit. Other suitable interface and software combinations might also be available.

The NetSC520 demonstration board also contains a BIOS configured specifically for the ÉlanSC520 microcontroller. The included BIOS allows the board to support most standard PC/AT functions via redirection of the command-line console to the serial port. (While a PC/104-Plus VGA adapter could be installed, the demonstration board does not have a keyboard interface, so console redirection is required for PC/AT operation.)

The board can run command-line based PC/AT-compatible operating systems (e.g., DOS and Linux) that support console redirection. You can configure the BIOS setup utility to start from a boot image that you provide on an attached IDE hard disk drive, or that you install in the board's Flash memory. (The selected boot device must already have the operating system installed and configured for console redirection.) For details on the included BIOS and other included software, see the online documentation provided with your kit.

For information on how to:

Setting Up the Board



CAUTION: As with all computer equipment, the NetSC520 demonstration board may be damaged by electrostatic discharge (ESD). Please take proper ESD precautions when handling any board.

Warning: Read before Using this Board

Before applying power, the following precautions should be taken to avoid damage or misuse of the board:

- Make sure the provided power supply is plugged into the board's power connector correctly. See "Power Supply" on page 2-16 for details.
- See "Top Layout of NetSC520 Demonstration Board" on page 2-3 for connector positions.
- Check the floppy disk or CD-ROM that was shipped with your kit for README or errata documentation. Read all the information carefully before continuing.

For current application notes, technical bulletins, and CodeKit software see the AMD World Wide Web page at **www.amd.com** and follow the link to Embedded Systems.

Installation Requirements

You need the following items (in addition to the board from the kit):

Required for AMDebug™ access:

- A Macraigor Systems LLC Raven-AMD device, or other suitable JTAG-compatible interface
- A PC running the included REMON monitor software, or other monitor/debugger software that supports the JTAG interface being used

> **NOTE:** This chapter assumes the Raven-AMD device and REMON software are used for AMDebug access. See the online documentation included with your kit, or the Embedded Processors, CodeKits section of **www.amd.com**, for the latest information about available board debugging techniques.

Required for redirected-console operation:

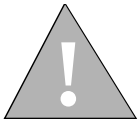
- An ANSI terminal or a PC running ANSI terminal emulation software
- A null-modem cable (included in kit)

To boot from a hard disk (or set up a resident Flash disk):

- An IDE-compatible hard disk drive
- AT-compatible operating system (preinstalled on the hard disk drive and configured for console redirection)

> **NOTE:** This chapter assumes MS-DOS is used for the installed operating system. See the online documentation included with your kit, or the Embedded Processors, CodeKits section of **www.amd.com**, for the latest information about operating systems that might be used.

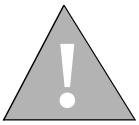
- A compact (notebook-style) 44-pin 2-mm-pitch hard-disk-drive cable (included in kit). The kit also includes a cable adapter in case your hard disk drive requires a 0.1-inch-pitch connector.



CAUTION: Use the configuration described here when you first start the demonstration board. Before using other features, read the appropriate sections in Chapter 2, "Board Functional Description."

Board Installation

NOTE: See Figure 2-1 on page 2-2 for a block diagram of the board. See Figure 2-2 on page 2-3 for a layout diagram of the board, including connector locations referenced in this section.



CAUTION: Make sure the demonstration board power supply is *not* plugged into an electrical outlet while setting up the board.

1. Remove the board from the shipping carton. Visually inspect the board to verify that it was not damaged during shipment. The following steps assume the board's jumpers are in the factory default configuration (settings are listed in "Jumper and Dip Switch Settings" on page A-1).
2. If you are preparing to use the AMDebug utility, perform the following steps:
   a. Connect the Macraigor Raven-AMD device to your PC using a parallel cable. This cable should be included with the Raven device.
   b. Make sure the board's Debug_Enter switch (S3, switch 1) is On.
   c. Apply power to the Raven device by plugging the supplied power cord first into the Raven device power supply, and then into an AC outlet.
   d. Attach the Raven device to the demonstration board's AMDebug port via the short 12-pin ribbon cable supplied. Orient pin 1 (the red stripe) away from the edge of the board.

      NOTE: Do not press the board's Reset switch with the Raven device attached. Instead use the REMON Z command to reset the board. If the board freezes with the Raven device attached, unplug the Raven device, then unplug the board's power adapter and plug it back in.

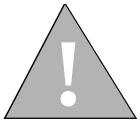
      Unlike other devices, the Raven device can be safely connected to the AMDebug port at any time, even if power is already applied to the demonstration board.
3. If you are setting up for redirected-console operation, connect the null-modem cable between the COM2 connector on the NetSC520 demonstration board (connector J7) and the appropriate serial port of your terminal or PC.

4. If you are installing a hard disk drive, perform the following steps:
    a. Inspect the 44-wire IDE ribbon cable. Note the red wire or any other marking that indicates wire 1 on the cable.
    b. Connect one end of the 44-wire IDE cable to the hard disk drive. The connector's orientation should be indicated in the drive documentation, or marked near the connector on the drive. Usually wire 1 is oriented towards the drive's power cable connector.
    c. Connect the other end of the 44-wire IDE cable to the 44-pin IDE connector (connector J1) on the demonstration board (orient wire 1 away from the PIO LEDs). See Figure 2-2 on page 2-3 for the connector location.

Using the AMDebug™ Technology

Use the following steps to access the NetSC520 demonstration board via the Macraigor Raven-AMD device and the included REMON software.

1. Make sure you have installed the NetSC520 demonstration board correctly as described in “Setting Up the Board” on page 1-2.
2. If you have not already done so, install the included REMON software on the attached PC. See the REMON software documentation for details.
3. If you have not already done so, apply power to the demonstration board by plugging the supplied AC adapter first into connector J8 on the board, and then into an AC outlet.



CAUTION: Failure to use the correct AC adapter can damage the NetSC520 demonstration board.

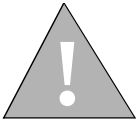
4. Open an MS-DOS prompt on the attached PC. (If you are not familiar with DOS commands, type HELP and press Enter for command help.)
5. In the MS-DOS prompt, CD to the directory containing the REMON software.
6. Type `REMON` and press Enter. The REMON welcome message is displayed, followed by the `REMON>` prompt.
7. Type `Z` and press Enter to reset the NetSC520 demonstration board. The LEDs near the Ethernet connector should flash briefly when the board resets.
8. Type `Yn` and press Enter to initialize the NetSC520 demonstration board. The LEDs near the AMDebug connector should change during initialization.

Applications can be loaded into either Flash memory or SDRAM. Refer to the online documentation in your kit for details about using REMON, and for information about other software included with the kit. Also refer to the Embedded Processors, CodeKits section of **www.amd.com** for related CodeKit software and documentation.

Starting from an IDE Hard Disk

Use the following steps to start up the NetSC520 demonstration board from an IDE hard disk on which you have preinstalled an operating system (while the disk was connected to another PC).

1. Make sure you have installed the NetSC520 demonstration board correctly as described in “Setting Up the Board” on page 1-2.
2. Configure your ANSI terminal or terminal emulation software with the following settings:
   - 9600 bits/s
   - 8 data bits
   - No parity
   - 1 stop bit
3. Apply power to the demonstration board by plugging the supplied AC adapter first into connector J8 on the board, and then into an AC outlet.



CAUTION: Failure to use the correct AC adapter can damage the NetSC520 demonstration board.

   Various LEDs on the board should light, and the terminal should start displaying startup information.
4. As the system starts, follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system’s date, time, startup drive, and other options (if necessary).
5. In the BIOS setup utility, use the automatic configuration option to set up Drive C and select it as the boot device. Select either physical addressing or logical block addressing (LBA) as appropriate for your hard disk drive.

   For more information on the included BIOS, see the online BIOS manual included with your kit.
6. Save and exit the setup utility.
7. The system should now boot using the operating system on the hard disk. If you encounter any problems, see “Installation Troubleshooting” on page 1-10.

Starting from Flash Memory

The demonstration board can be set up with a bootable resident flash disk (RFD) as drive A (768 Kbytes). An additional bootable drive C (14 Mbytes) can also be set up.

Setting Up RFD Drive A:

1. Make sure you have installed the NetSC520 demonstration board correctly as described in “Setting Up the Board” on page 1-2.
2. Use the steps in “Starting from an IDE Hard Disk” on page 1-7 to start the system with an MS-DOS boot image. Make sure the boot image includes the FORMAT.COM program.
3. As the system starts, follow the instructions shown on the screen to enter the BIOS setup utility.
4. In the BIOS setup utility, set up Drive A to be a “768K Soft RFD.” *Do not* change the drive C configuration; leave drive C as the startup disk. Save the BIOS settings and start the board using the IDE hard disk drive C.
5. At the MS-DOS prompt, type **FORMAT /S A:** and press Enter. This formats the RFD A drive and makes it bootable.
6. Copy any additional software that you require to the RFD A drive. If you intend to set up an RFD C drive, be sure to copy FDISK.EXE and FORMAT.COM to the A drive.
7. After all disk activity stops, reset the demonstration board (press the Reset button on the board) and enter the setup utility again.
8. In the BIOS setup utility, select drive A as the boot drive and save settings. You can now remove power and disconnect the IDE hard disk drive if desired.
9. Power up or restart the demonstration board.

The system should now boot from the DOS RFD just like a standard PC. If you encounter any problems, see “Installation Troubleshooting” on page 1-10.

Setting Up RFD Drive C:

1. Make sure you have installed the NetSC520 demonstration board correctly as described in “Setting Up the Board” on page 1-2.
2. Use the steps in “Setting Up RFD Drive A:” on page 1-8 to set up and start the system with RFD drive A. Make sure the boot image on drive A includes the FDISK.EXE and FORMAT.COM programs.
3. As the system starts, follow the instructions shown on the screen to enter the BIOS setup utility.
4. In the BIOS setup utility, set up Drive C to be a “14MB Hard RFD.” *Do not* change the drive A configuration; leave drive A as the startup disk. Save the BIOS settings and start the board using the RFD drive A.
5. At the MS-DOS prompt use the **FDISK** program to partition the new 14 Mbyte RFD device. (Note that FDISK uses screen attributes not available on the redirected display. This makes the program somewhat difficult to use, but is normal.)
6. After the partition is created, reset the demonstration board (press the Reset button on the board) and wait for the MS-DOS prompt to be displayed.
7. At the MS-DOS prompt, type **FORMAT /S C:** and press Enter to format the RFD C drive and make it bootable.
8. Copy any additional software that you require to the RFD C drive.
9. After all disk activity stops, reset the demonstration board (press the Reset button on the board) and enter the setup utility again.
10. In the BIOS setup utility, select drive C as the boot drive and save settings. Reset the demonstration board again.

The system should now boot from the DOS RFD drive C. If you encounter any problems, see “Installation Troubleshooting” on page 1-10.

NOTE: This chapter assumes MS-DOS is used for the installed operating system. See the online documentation included with your kit, or the Embedded Processors, CodeKits section of **www.amd.com**, for the latest information about operating systems that might be used.

Installation Troubleshooting

Table 1-1. Installation Troubleshooting

Problem	Solution
The power LEDs on the back of the board remain dark after I plug in the power adapter.	Make sure the correct AC power adapter is plugged in and correctly attached to the board.
The power LEDs on the back of the board light, but the PIO LEDs near the AMDebug port remain dark.	Make sure all cables and adapters are connected properly. If the Raven device is not attached, press Reset (S4). If you pressed Reset (S4) with the Raven device attached, remove the Raven device; then unplug the power adapter and plug it back in. (When the Raven device is attached, use REMON's Z command to reset the board.) If the problem persists, the board's Flash memory might be corrupted. Use REMON and the NetSC520 BIOS CodeKit to reinstall the Flash memory contents.
The PIO LEDs flash and display a pattern, but I see nothing on the redirected console display.	Make sure all cables and adapters are connected properly, and the CMOS battery is correctly installed. Make sure your terminal or terminal emulator supports ANSI and is configured correctly (8, N, 1, 9600 baud). Make sure you are using a null-modem cable, connected to the correct port on your terminal and to the NetSC520 demonstration board's COM2 port (part J7) If the problem persists, invalidate the CMOS RAM by temporarily removing the battery. Wait a few seconds, then reinstall the battery. This makes it necessary to run Setup and restore startup settings, but it also clears any corrupted settings that might be present. If the problem still persists, the board's Flash memory might be corrupted. Use REMON and to reinstall the included BIOS software.

Table 1-1. Installation Troubleshooting (Continued)

Problem	Solution
I see the startup information on the monitor but it says there's a battery problem or CMOS checksum error and the system doesn't finish booting.	Follow the BIOS instructions to run the Setup utility to configure the CMOS RAM and save settings.
I configured the CMOS RAM and saved my settings, but settings are lost the next time I turn on the NetSC520 demonstration board.	Make sure a fresh 3.0-V 12-mm coin cell is installed correctly ("+" side facing up) in the BT1 battery holder.
I get a "Missing Keyboard" error message on the monitor during boot-up.	This might happen if you install a PC/104-Plus VGA adapter and attempt to boot an operating system not configured for console redirection. While a VGA adapter might be used for display, the NetSC520 demonstration board does not have a PC/AT keyboard interface; therefore, the board can only be operated via console redirection or the AMDebug port.
The BIOS debugging monitor prompt is displayed.	Check that any PC/104-Plus devices are installed correctly and known to be functional.
I have installed a hard disk with a preinstalled operating system, but the NetSC520 demonstration board won't access the hard disk.	Check that the 44-wire IDE cable is properly connected at both the drive end and the board end (board connector J14 at location M1). Double-check the Pin 1 orientation. If the drive requires a separate power supply, make sure the supply is connected properly and turned on. Check that the CMOS setup is configured correctly for the drive. Make sure the drive functions properly on a different system.
There is a problem I cannot resolve.	Check that the board is set to its default settings (see Appendix A, "Jumper and Dip Switch Settings"). Contact the AMD Technical Support Hotline (see page iii).

Chapter 2

Board Functional Description

The NetSC520 demonstration board shows how easy it is to create a low-cost, embedded Ethernet solution using the ÉlanSC520 microcontroller and the AMD Am79C973 PCnet-*FAST III* Ethernet controller. In addition to the microcontroller and Ethernet controller, the NetSC520 demonstration board contains two Am29LV641D 8-Mbyte Flash memory chips and two 8-Mbyte SDRAM chips.

Read the following sections to learn more about the NetSC520 demonstration board hardware:

Block Diagram

Figure 2-1 shows a block diagram of the NetSC520 demonstration board.

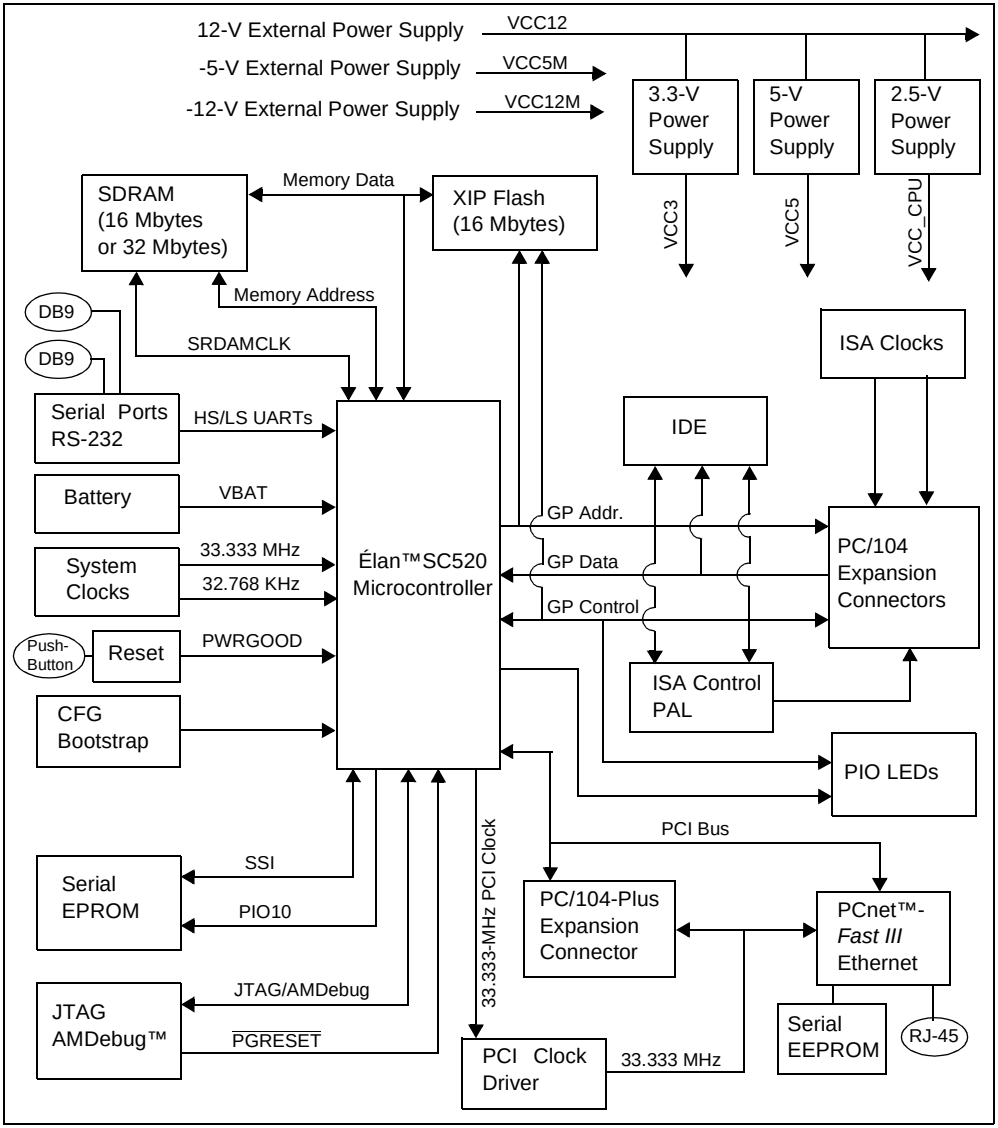


Figure 2-1. NetSC520 Demonstration Board Block Diagram (Same as Figure 0-1.)

Board Layout

Figure 2-2 shows the top board layout of the NetSC520 demonstration board. The bottom layout is shown in Figure 2-3 on page 2-4.

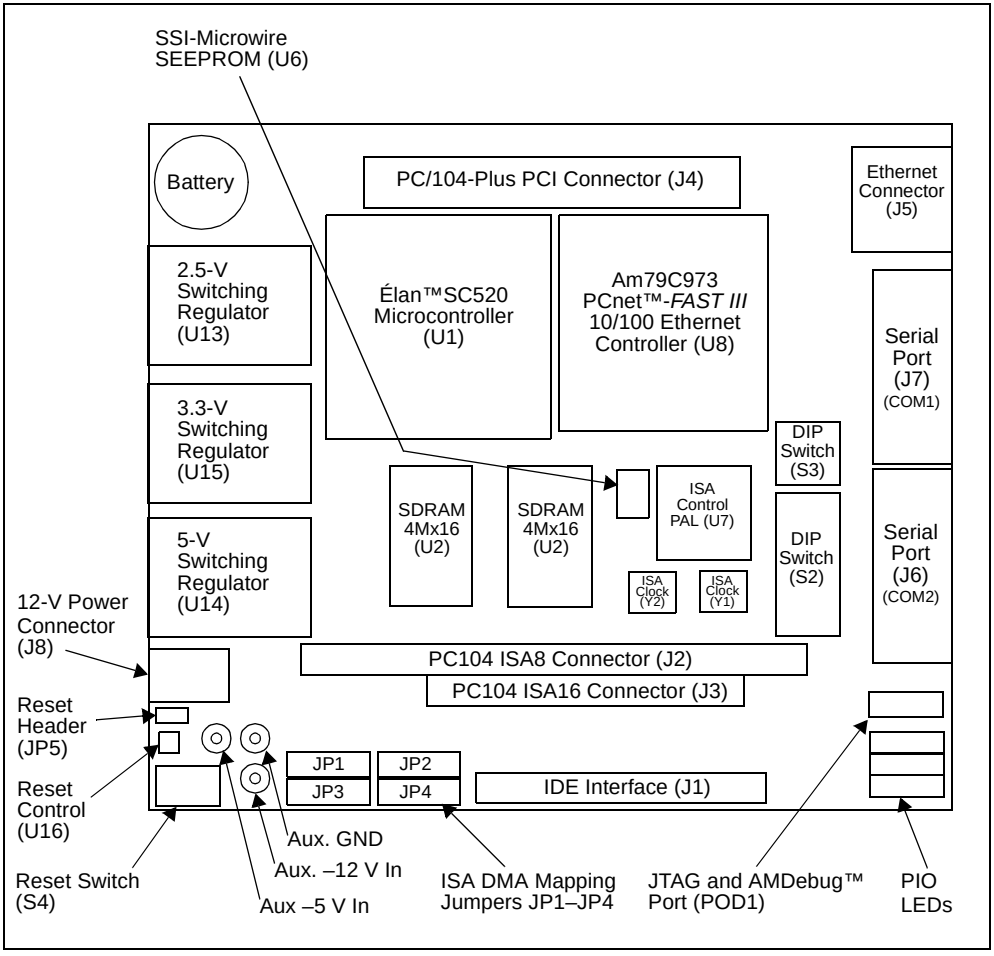


Figure 2-2. Top Layout of NetSC520 Demonstration Board

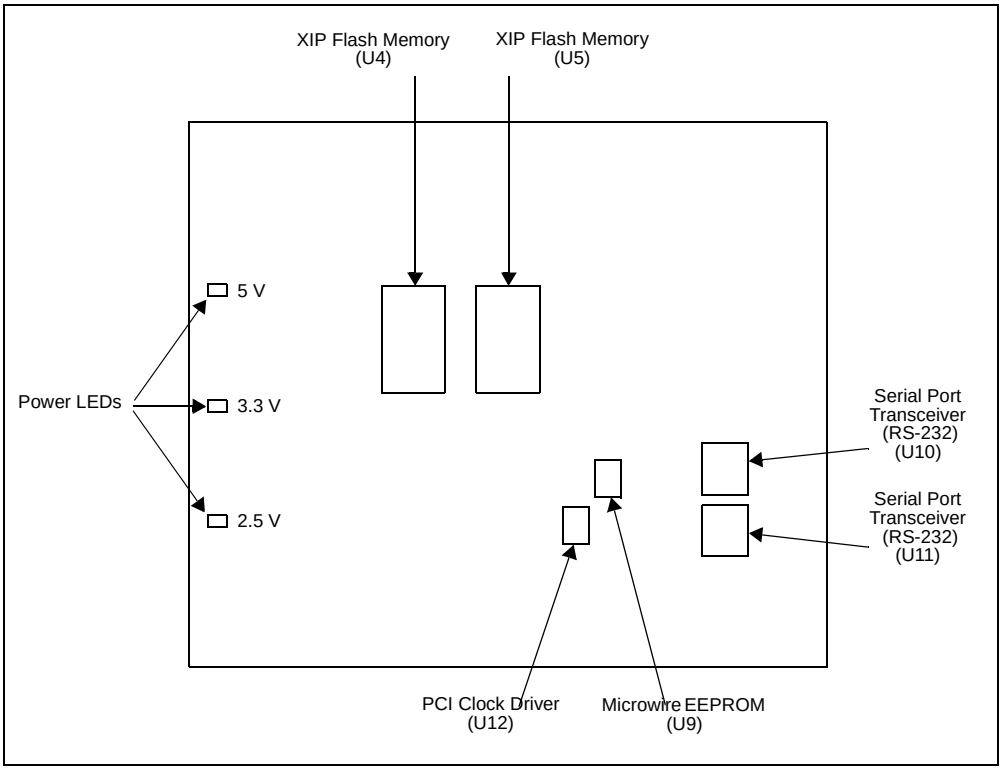


Figure 2-3. Bottom Layout of NetSC520 Demonstration Board

Descriptions

The following sections describe the features and functions of the NetSC520 demonstration board. For additional information about the demonstration board, refer to the following sections:

Appendix A, “Jumper and Dip Switch Settings” explains how to set up the board’s various jumpers and switches.

Appendix B, “Board Routing Rules” provides information useful in laying out designs similar to the NetSC520 demonstration board.

For component layout and locations, refer to Figure 2-2 on page 2-3 and Figure 2-3 on page 2-4.

Élan™SC520 Microcontroller

The ÉlanSC520 microcontroller is a full-featured microcontroller developed for the general embedded market. Designed for medium- to high-performance applications in the telecommunications, data communications, and information appliance markets, the ÉlanSC520 microcontroller is particularly well suited for applications requiring high throughput combined with low latency, low chipcount, and low cost.

The ÉlanSC520 microcontroller utilizes a high-performance, industry-standard, 33-MHz, 32-bit PCI bus for high-bandwidth I/O peripherals. The microcontroller also contains a simple 8- and 16-bit general-purpose (GP) bus for a glueless connection to low-bandwidth peripherals. The GP bus supports most legacy ISA peripherals.

The ÉlanSC520 microcontroller utilizes the industry-standard x86 architecture instruction set that enables compatibility across a variety of performance levels from the low-end 16-bit Am186 processors to the high-end AMD-K6™E family processors. Software written for the x86 architecture family is compatible with the ÉlanSC520 microcontroller.

With the AMDebug technology, the ÉlanSC520 microcontroller provides a full-featured, high-performance in-circuit emulation capability that enables you to test and debug your software earlier in the design cycle.

In addition to these features, the ÉlanSC520 microcontroller provides a high-performance SDRAM controller, ROM/Flash controller, flexible address-mapping hardware, 8- and 16-bit general-purpose (GP) bus interface, clock generation, integrated peripherals, JTAG boundary scan test interface, and various system test and debug features.

For more information about the ÉlanSC520 microcontroller, refer to the *Élan™SC520 Microcontroller Data Sheet*, *Élan™SC520 Microcontroller User's Manual*, and *Élan™SC520 Microcontroller Register Set Manual*, which are included in your kit.

10/100BaseT Ethernet Controller

The NetSC520 demonstration board contains the AMD Am79C973 PCnet-*FAST III* Ethernet controller chip. The high-performance 10/100BaseT Ethernet port enables the NetSC520 demonstration board to connect to a high-bandwidth LAN. In this design, a compact yet complete full-duplex implementation is achieved by wiring the Ethernet chip's built-in transceiver (PHY) to a special RJ-45 10/100BaseT connector that incorporates the required magnetics, plus link/speed LEDs. Of course, the Am79C973 could also be used with separate discrete magnetics and connector components.

The Am79C973 device logically resides on the PCI bus and is wired for full bus-mastering capability. The PCI address bit 24 is used for the IDSEL pin of the Am79C973 device (it is Device D in the PCI configuration space). The Am79C973 registers can be configured by either the PCI configuration space mechanism, or by downloading the configuration information from a dedicated 1-Kbit serial EEPROM (part U9) connected to the Ethernet chip. Software is provided to read the chip's media access code (MAC) and access its configuration.

Figure 2-4 shows a block diagram of the 10/100BaseT Ethernet.

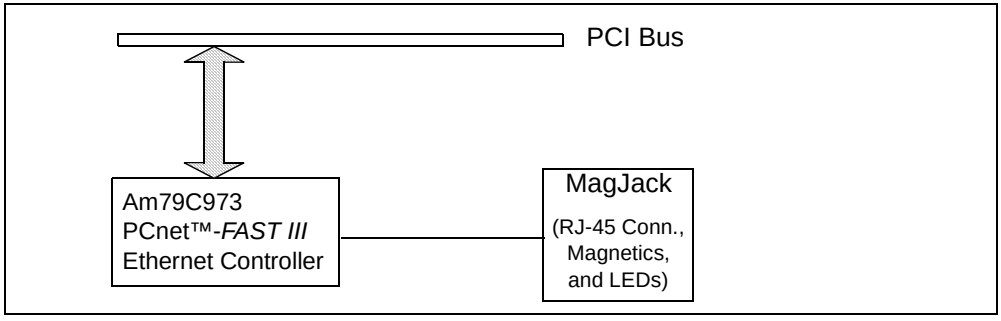


Figure 2-4. On-Board 10/100 Mbit/s Ethernet Controller Block Diagram

PC/104-Plus Expansion Interface

The NetSC520 demonstration board provides a set of PC/104-Plus connectors (parts J2, J3, and J4) to allow the installation of a wide array of interface devices. These can include standard devices such as video, sound, SCSI, or PCMCIA adapters, or diagnostic devices such as bus analyzers and other diagnostic hardware. For more information about the PC/104-Plus interface, see **www.pc104.org**.

The PC/104-Plus interface supports up to four attached devices, which can use either PCI bus or ISA-compatible signaling. However, the ISA-compatible signals on the demonstration board are not buffered, so no more than two devices should use ISA signaling, or one device if the IDE connector is also used.

The PC/104-Plus interface is implemented via the ÉlanSC520 microcontroller's PCI and GP-bus interfaces, with additional ISA-compatible signals ($\overline{\text{SMEMR}}$ and $\overline{\text{SMEMWR}}$) generated by programmable logic (device U7).

For PCI bus configuration, PC/104-Plus devices are addressed as PCI Devices 9, A, B, and C (their IDSELx lines are connected to PCI address lines AD20–AD23, respectively). PCI-V2.2-compliant peripheral devices are supported, including PCI masters.The ÉlanSC520 microcontroller's PCI output signals use 3.3-V signaling; the input signals accommodate 3.3-V or 5-V signaling.

Jumpers selections are required to route the DMA request and acknowledge lines used by the ISA portion of the PC/104-Plus interface. For details, see "ISA DMA Selection" on page A-1.

Several of the microcontroller's GPIRQ lines are multiplexed with the PIO-controlled LED signals, as shown on sheet 13 of the schematics (included as a separate document in your kit). If any attached device is to use one of these GPIRQ lines, it is necessary to first depopulate the zero-ohm resistor that connects that line to the associated LED.

Expansion Power Supply

The PC/104-Plus connectors provide +5-V and +3.3-V power supply lines. The PC/104-Plus –5-V and –12-V supplies are not provided; however, miniature banana jacks are provided on the board so that an external supply can be used to provide those voltages. The jacks are color coded Red for –5 V, White for –12 V, and Black for the supply's Ground connection.

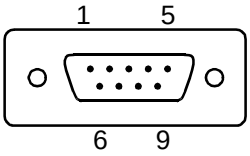
The power budget for the PC/104-Plus connectors has not been determined. However, the onboard voltage regulators' capacity is more than adequate for the board itself. A conservative PC/104-Plus current limit of 3 A for either 3.3 V or 5 V should be safe.

Serial Ports (RS-232)

The NetSC520 demonstration board provides two onboard RS-232 serial ports (J6 and J7) that are controlled by the ÉlanSC520 microcontroller. The serial ports are equipped with DB-9 Data Terminal Equipment (DTE) connectors. The pin assignment for the DB-9 connectors is shown in Figure 2-5. For serial port connector locations, refer to Figure 2-2 on page 2-3.

Traditionally, PCs also have Data Terminal Equipment (DTE) ports. A null modem cable or adapter (provided in kit) is required to connect a DTE port with a DTE port.

The RS-232 specification calls for signals that are driven at non-CMOS levels. Single-chip RS-232 driver/receiver devices (U10 and U11) are used to convert to and from the required voltages.



Notes:

The included BIOS maps COM1 to connector J6 and COM2 to connector J7. See Figure 2-2 on page 2-3 for connector locations.

Figure 2-5. Serial Port Connector Pins

Table 2-1. Serial Port Pin/Signal Table

Connector Pin	Signal
1	$\overline{\text{DCD}}$
2	RXD
3	TXD
4	$\overline{\text{DTR}}$
5	GND

Connector Pin	Signal
6	$\overline{\text{DSR}}$
7	$\overline{\text{RTS}}$
8	$\overline{\text{CTS}}$
9	$\overline{\text{RI}}$

Memory

The memory on the NetSC520 demonstration board consists of SDRAM and Flash memory.

SDRAM

The NetSC520 demonstration board consists of two, 4-Mbit by 16-bit SDRAM devices for a total of 16 Mbytes. A similar design could provide 32 Mbytes by populating higher-capacity SDRAM chips with the same footprint.

XIP Flash Memory

The on-board execute-in-place (XIP) Flash memory uses two AMD Am29LV641D devices (U4 and U5) configured as a single bank of 16 Mbytes in a 32-bit data width, and selected via the ÉlanSC520 microcontroller's $\overline{\text{BOOTCS}}$ signal.

The XIP Flash memory comes with BIOS software specifically designed for this demonstration board. See the included online documentation for details about the BIOS software.

Memory Maps

The memory maps shown in Table 2-2 and Table 2-3 on page 2-12 are typically used when accessing the demonstration board.

The user is free to specify any Flash memory map when running custom embedded applications, except that the reset vector is always at offset 00FFFFF0h in Flash memory, and Real mode after the first far jump can only access the lower 1 Mbyte of Flash memory. See the SDRAM size CodeKit, CK0031, for more information.

Table 2-2. REMON Memory Map (YN Command)

Address Range	Function
FFFEF000–FFFEFFFF	ÉlanSC520 microcontroller memory-mapped configuration register (MMCR) area
04000000–04FFFFFF	16 Mbyte Flash memory
00000000–00FFFFFF	16 Mbyte SDRAM

Table 2-3. BIOS Memory Map

Address Range	Function	
02000000–02FFFFFF	16 Mbyte Flash memory:	
	02FC0000–02FFFFFF	High BIOS image
	02F00000–02FBFFFF	768-Kbyte soft RFD (if configured)
	02100000–02EFFFFF	14-Mbyte hard RFD (if configured)
	020C0000–020FFFFF	Low BIOS image
	02000000–020BFFFF	Available for system and applications
000DF000–000DFFFF	ÉlanSC520 microcontroller memory-mapped configuration register (MMCR) overlay	
00000000–00FFFFFF	16 Mbyte SDRAM	

AMDebug™ Technology and JTAG Port

The ÉlanSC520 microcontroller's AMDebug technology interface provides a low-cost, full-featured, in-circuit emulation capability. This in-circuit emulation support was developed at AMD specifically to enable users to test and debug their software early in the design cycle.

The NetSC520 demonstration board uses the serial AMDebug technology connection, which is based on an enhanced JTAG protocol and an inexpensive 12-pin 2-mm pitch connector (POD1).

The AMDebug technology allows the demonstration board to be controlled independently of any software installed on the board, via a JTAG-compatible debugging interface such as the Macraigor Systems LLC Raven-AMD device. The Raven device provides typical monitor/debugger functionality on an attached PC running the REMON software included with your kit. Other suitable interface and software combinations might also be available. Depending on the software used, available functions can include:

- Trace and debug cache memory
- Single-step program execution
- Read and write processor registers
- Program the Flash memory

See "Using the AMDebug™ Technology" on page 1-6 and "Memory" on page 2-11 for related information. See also the online documentation provided with the kit.

Serial EEPROM

A separate 1-Kbit Microwire serial EEPROM (U6) is provided for general-purpose storage of configuration information. (This is in addition to the Ethernet configuration EEPROM, part U9, see "10/100BaseT Ethernet Controller" on page 2-7.)

The general-purpose serial EEPROM is connected directly to the ÉlanSC520 microcontroller's synchronous serial interface (SSI). Software to read and write the serial EEPROM is provided in the kit. See the kit's online documentation for details.

IDE Hard Disk Connector

The demonstration board provides one 2-mm pitch IDE connector. The connector used is intended for 2.5-inch hard disk drives. Your kit includes the necessary 2-mm pitch cable, as well as an adapter for connecting 0.1-inch pitch IDE devices. An LED (part D1) is provided near the IDE connector to indicate IDE activity.

The IDE interface is implemented via the ÉlanSC520 microcontroller's GP-bus. The IDE device can generate interrupts on GPIRQ10. The interrupt's mapping can be changed by reprogramming the microcontroller.

The IDE connector supports one master and one slave device. If only one device is attached to the IDE connector, that device must be configured as an IDE master. If a two-position cable is used to attach two devices to the IDE connector on the board, one of the devices must be configured as an IDE master and the other as an IDE slave. See each IDE device's documentation for configuration details.

NOTE: Any current required by an attached IDE device must be considered when attaching PC/104-Plus expansion devices. See "Expansion Power Supply" on page 2-9

PIO-Controlled LED Indicators

A group of nine LEDs (D21–D29) are used to indicate activity on a subset of the ÉlanSC520 microcontroller's Programmable I/O (PIO) signals. Table 2-4 shows which PIO signal is represented by each LED. Positions are shown with the board's corner to the lower-right.

Table 2-4. PIO LED Indicator Interface

Color	Position in Group	LED Part #	Resistor Part #	PIO Pin Name
Red		D25	R87	PIO17 [GPIRQ6]
		D28	R92	PIO20 [GPIRQ3]
		D22	R80	PIO23 [GPIRQ0]
Yellow		D27	R91	PIO16 [GPIRQ7]
		D21	R79	PIO19 [GPIRQ4]
		D24	R84	PIO22 [GPIRQ1]
Green		D29	R94	PIO6
		D23	R83	PIO18 [GPIRQ5]
		D26	R88	PIO21 [GPIRQ2]

NOTE: Several of the microcontroller's GPIRQ lines are multiplexed with the PIO-controlled LED signals. If any attached device is to use one of these GPIRQ lines, it is necessary to first depopulate the zero-ohm resistor that connects that line to the associated LED, as shown in Table 2-4 and on sheet 13 of the schematics (included as a separate document in your kit).

Power Supply

The NetSC520 demonstration board is powered by a single power connector (part J8) with the following specifications:

- +12 V DC
- 4.0 A maximum current
- Barrel connector, 5.5-mm outside diameter, 2.5-mm inside diameter
- Center-positive barrel plug

CAUTION: Check the AC adapter voltage, polarity, and current ratings before connecting it to the board. Using an incorrect adapter can damage the board or the power supply.

The provided AC adapter is capable of providing power for the board and as many PC/104-Plus add-on cards as the onboard voltage regulators can supply (see “Expansion Power Supply” on page 2-9). The AC adapter supports input power voltages of 100–250 V AC at 47–63 Hz.

Onboard regulation is provided for the board’s 2.5-V (CPU), 3.3-V, and 5-V requirements. LEDs D20, D17, and D16, respectively, indicate power-on status for each of these supplies. (The power LEDs are located on the back of the board.) Each regulator is capable of supplying 4.5 A of current at its output voltage.

NOTE: The design of the onboard power supplies was selected for rapid development. These supplies are not intended to be examples of optimal power-supply design.

Power for the PC/104-Plus –5-V and –12-V supplies is not provided; however, miniature banana jacks are provided on the board so that an external supply can be used to provide those voltages. The jacks are color-coded Red for –5 V, White for –12 V, and Black for the supply’s Ground connection.

RTC Backup Battery

A 12-mm 3-V coin cell in battery holder BT1 provides backup power for the ÉlanSC520 microcontroller’s RTC clock and CMOS configuration whenever external power is removed from the board.

Reset Control

System reset control is provided by a Micrel MC8114 reset controller (part U16). Push-button switch S4 and header JP5 are provided for user-initiated resets. Header JP5 is wired in parallel with switch S4 so that an external reset switch can be attached, if needed.

The board can also be reset under software control or via the AMDebug port.

Appendix A

Jumper and Dip Switch Settings

This appendix contains the jumper and DIP switch settings for the NetSC520 demonstration board.

Jumper Settings

The following information provides the jumper settings and pin locations for the various jumpers.

ISA DMA Selection

The ÉlanSC520 microcontroller supports two DMA channels via its GPDRQ0, GPDACK0, GPDRQ1, and GPDACK1 signals. The ISA-compatible signaling on the PC/104-Plus interface provides paths for seven DMA channels (0–3 and 5–7), which are shared by attached devices. Jumpers JP1, JP2, JP3, and JP4 allow you to route any one ISA-bus DMA channel to either of the microcontroller's two DMA channels. Figure A-1 shows the pin numbering for these jumpers.

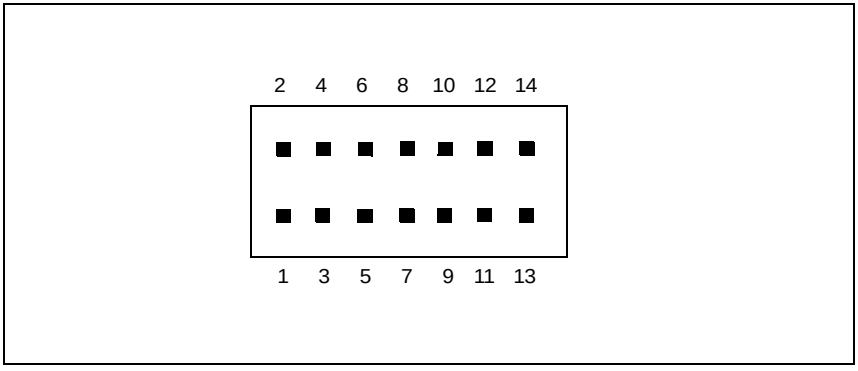


Figure A-1. Jumper JP1, JP2, JP3, and JP4 Pin Numbering

Jumper JP1

Jumper JP1 is used to route one ISA-compatible DRQn channel from the PC/104-Plus connector to the microcontroller's GPDRQ0 input. The following settings indicate the possible configurations for jumper JP1.

- To route ISA DRQ0 to microcontroller GPDRQ0, jumper pins 1 and 2.
- To route ISA DRQ1 to microcontroller GPDRQ0, jumper pins 3 and 4.
- To route ISA DRQ2 to microcontroller GPDRQ0, jumper pins 5 and 6.
- To route ISA DRQ3 to microcontroller GPDRQ0, jumper pins 7 and 8.
- To route ISA DRQ5 to microcontroller GPDRQ0, jumper pins 9 and 10.
- To route ISA DRQ6 to microcontroller GPDRQ0, jumper pins 11 and 12.
- To route ISA DRQ7 to microcontroller GPDRQ0, jumper pins 13 and 14.

Jumper JP2 must be used to route the corresponding $\overline{\text{DACKx}}$ signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP3 and JP4 (if any). Figure A-2 shows the signal routing for jumper JP1, with ISA DRQ1 routed to GPDRQ0.

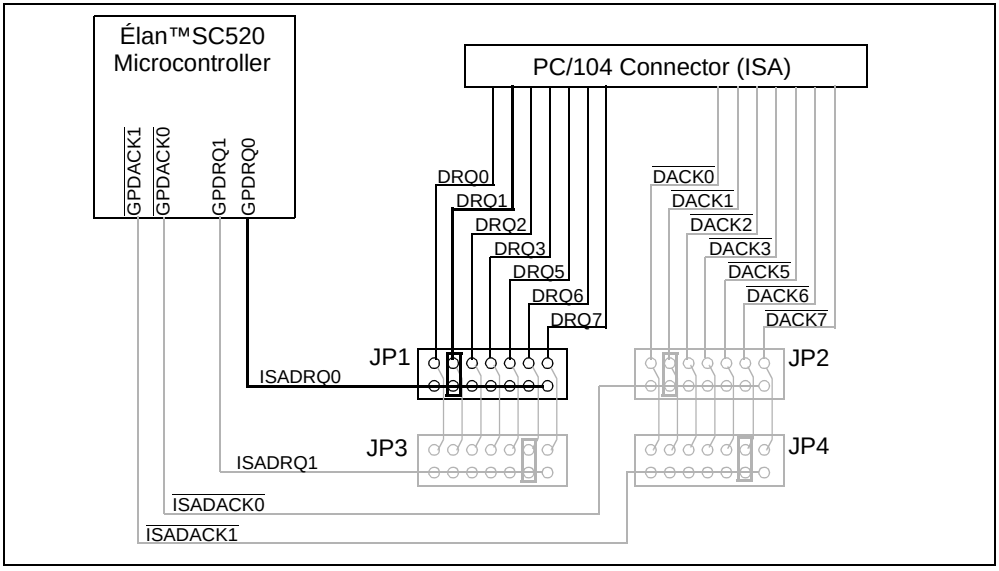


Figure A-2. Jumper JP1 Routing Example

Jumper JP2

Jumper JP2 is used to route one ISA-compatible $\overline{\text{DACKn}}$ channel from the PC/104-Plus connector to the microcontroller's $\overline{\text{GPDACK0}}$ input. The following settings indicate the possible configurations for jumper JP2.

- To route ISA $\overline{\text{DACK0}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 1 and 2.
- To route ISA $\overline{\text{DACK1}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 3 and 4.
- To route ISA $\overline{\text{DACK2}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 5 and 6.
- To route ISA $\overline{\text{DACK3}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 7 and 8.
- To route ISA $\overline{\text{DACK5}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 9 and 10.
- To route ISA $\overline{\text{DACK6}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 11 and 12.
- To route ISA $\overline{\text{DACK7}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 13 and 14.

Jumper JP1 must be used to route the corresponding DRQx signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP3 and JP4 (if any). Figure A-3 shows the signal routing for jumper JP2, with ISA $\overline{\text{DACK1}}$ routed to $\overline{\text{GPDACK0}}$.

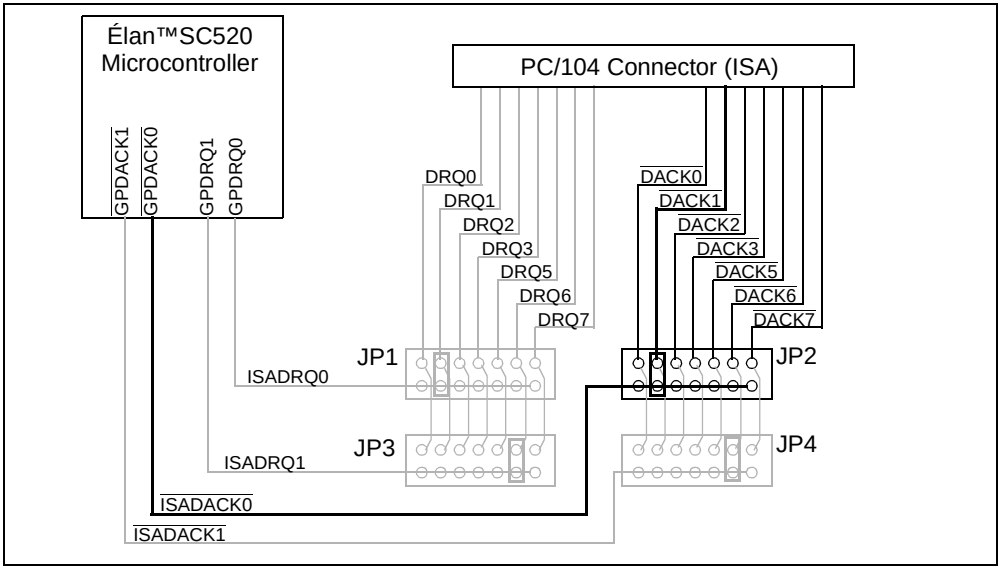


Figure A-3. Jumper JP2 Routing Example

Jumper JP3

Jumper JP3 is used to route one ISA-compatible DRQn channel from the PC/104-Plus connector to the microcontroller's GPDRQ1 input. The following settings indicate the possible configurations for jumper JP3.

- To route ISA DRQ0 to microcontroller GPDRQ1, jumper pins 1 and 2.
- To route ISA DRQ1 to microcontroller GPDRQ1, jumper pins 3 and 4.
- To route ISA DRQ2 to microcontroller GPDRQ1, jumper pins 5 and 6.
- To route ISA DRQ3 to microcontroller GPDRQ1, jumper pins 7 and 8.
- To route ISA DRQ5 to microcontroller GPDRQ1, jumper pins 9 and 10.
- To route ISA DRQ6 to microcontroller GPDRQ1, jumper pins 11 and 12.
- To route ISA DRQ7 to microcontroller GPDRQ1, jumper pins 13 and 14.

Jumper JP4 must be used to route the corresponding $\overline{\text{DACKx}}$ signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP1 and JP2 (if any). Figure A-4 shows the signal routing for jumper JP3, with ISA DRQ6 routed to GPDRQ1.

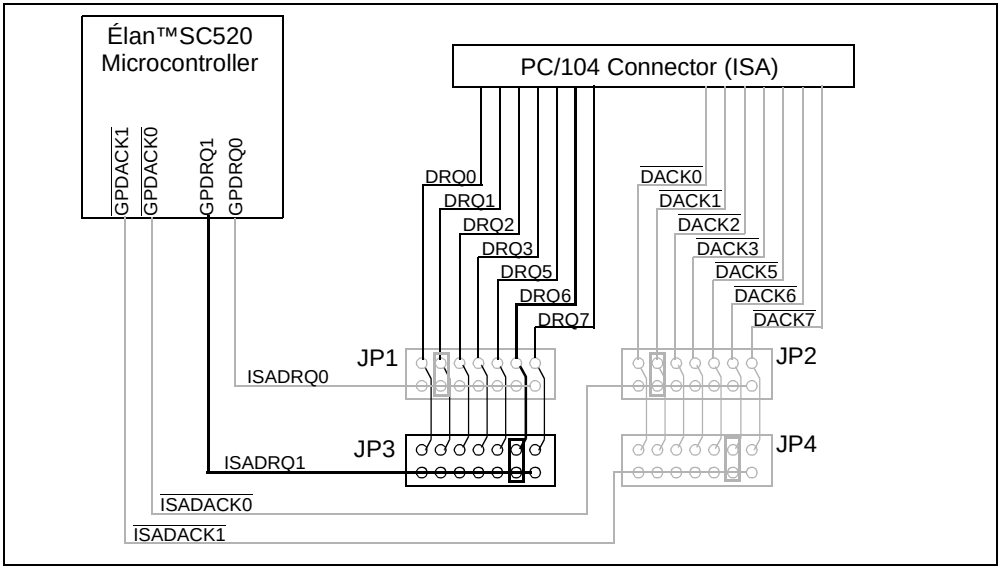


Figure A-4. Jumper JP3 Routing Example

Jumper JP4

Jumper JP4 is used to route one ISA-compatible $\overline{\text{DACKn}}$ channel from the PC/104-Plus connector to the microcontroller's $\overline{\text{GPDACK1}}$ input. The following settings indicate the possible configurations for jumper JP4.

- To route ISA $\overline{\text{DACK0}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 1 and 2.
- To route ISA $\overline{\text{DACK1}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 3 and 4.
- To route ISA $\overline{\text{DACK2}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 5 and 6.
- To route ISA $\overline{\text{DACK3}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 7 and 8.
- To route ISA $\overline{\text{DACK5}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 9 and 10.
- To route ISA $\overline{\text{DACK6}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 11 and 12.
- To route ISA $\overline{\text{DACK7}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 13 and 14.

Jumper JP3 must be used to route the corresponding DRQx signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP1 and JP2 (if any). Figure A-5 shows the signal routing for jumper JP4, with ISA $\overline{\text{DACK6}}$ routed to $\overline{\text{GPDACK1}}$.

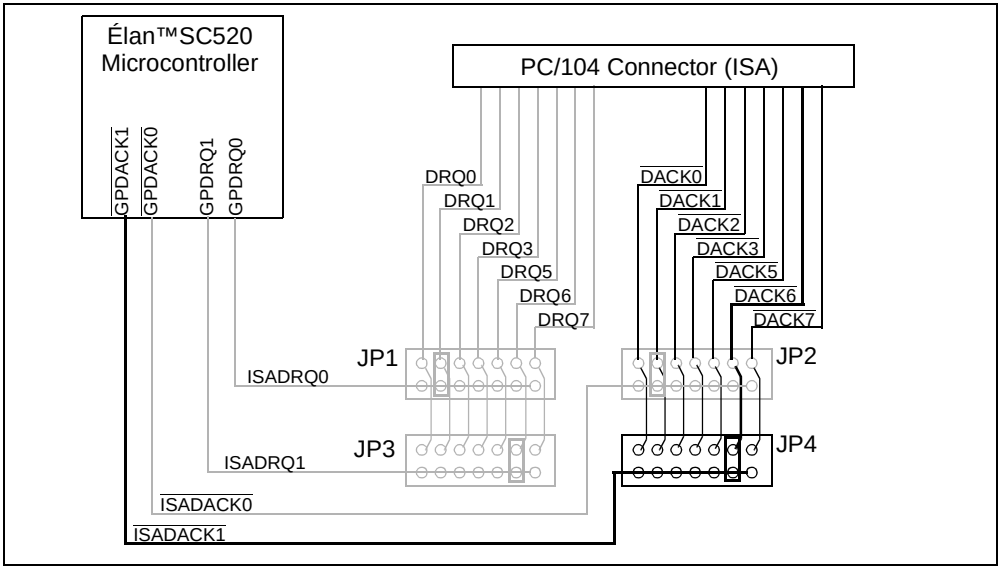


Figure A-5. Jumper JP4 Routing Example

Header JP5

Header JP5 is provided for connecting an external reset switch, if needed. See “Reset Control” on page 2-17.

DIP Switch Settings

This section provides the switch settings for the three DIP switches.

DIP Switch S2

Switch S2 is an eight-circuit DIP switch provided for software-defined boot configuration. Each switch is connected to one of the RSTLD[0–7] pins on the ÉlanSC520 microcontroller, which are sampled upon reset or power-up and stored in an internal register for software to read (see the *Élan™SC520 Microcontroller User's Manual* for details). These can be used by software to determine different modes of operation based on the switch settings.

The included BIOS uses switch segments S2-1 (RSTLD0) and S2-4 (RSTLD3); see the included online BIOS documentation for details. Signals not used by the BIOS can be used for any purpose. The default switch setting is shown in Figure A-6. For the location on the board, refer to "Board Layout" on page 2-3.

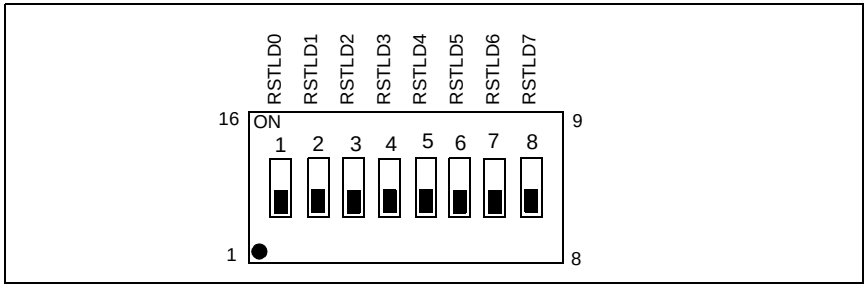


Figure A-6. DIP Switch S2 Default Setting

Table A-1. DIP Switch S2 Settings

Switch	Signal	Function
S2-1	RSTLD0	On enables Manufacturing mode (BIOS)
S2-2–S2-3	RSTLD1–RSTLD2	User-defined
S2-4	RSTLD3	On enables Safe mode (default BIOS setup)
S2-5–S2-8	RSTLD4–RSTLD7	User-defined

DIP Switch S3

Switch S3 is a three-circuit DIP switch used to select the ÉlanSC520 microcontroller AMDebug mode upon system startup. The default switch setting is shown in Figure A-7. A description of the DIP switch settings and functions are shown in Table A-2. For the board location, refer to “Board Layout” on page 2-3.

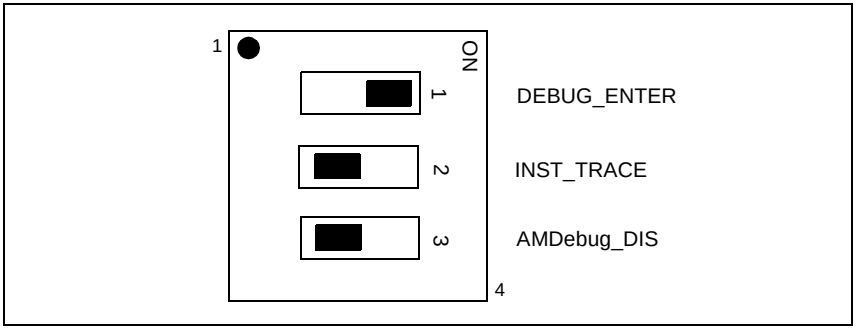


Figure A-7. DIP Switch S3 Default Setting

Table A-2. DIP Switch S3 Settings

Switch	Signal	Setting	Function
S3-1	DEBUG_ENTER	ON	Debug mode enabled
		OFF	Normal operation
S3-2	INST_TRACE	ON	Trace controller enabled (not armed, but ready to use)
		OFF	Normal operation
S3-2	AMDebug_DIS	ON	AMDebug technology always disabled
		OFF	Normal operation; AMDebug mode can be enabled by software.

Appendix B

Board Routing Rules

This appendix details the board routing rules that were used to lay out the NetSC520 demonstration board. This information should be useful as a guide for similar designs.

Trace Widths

Most signal routing on the board uses 0.005-inch trace width and 0.005-inch trace-to-trace spacing, except as otherwise noted. Clock nets are generally 0.005-inch trace width and 0.015-inch trace-to-trace spacing. Asynchronous control signals are 0.005-inch trace width and 0.010-inch trace-to-trace spacing. Power nets are 0.025–0.035-inch (minimum) trace width and 0.010–0.015-inch trace-to-trace spacing.

Power Distribution and Planes

The NetSC520 demonstration board has four ground and power planes: one split plane for VCC3 and VCC_CPU, one split plane for VCC5 and VCC12, and two GND planes. The board has six additional layers for signal routing.

Battery power, VCC5M, and VCC12M are each routed as wide trace on a signal layer. VCC12 is also routed as wide trace to most destinations on the board, except in the power supply section, where it is routed on a split section of the VCC5 plane. Another design could route VCC12 entirely as a wide trace on signal layers.

Two GND planes are used to make the printed circuit board symmetrical for easier manufacturing, and to help keep trace impedance the same on all layers. Earth_GND and Analog_GND are isolated ground networks that connect back to the main GND planes at a single point each. These isolated ground nets are routed as wide traces, but in another design they could be on a split ground plane, depending on what works best with the board placement and layout.

Signal Routing Order

Nearly all signals on the board involve the ÉlanSC520 microcontroller, so it is difficult to specify an exact routing order. After the microcontroller is routed, nearly all of the board is completed. However, this section provides some guidelines to follow.

Good power and clock distribution are essential to get any board to run reliably, so those nets should be connected first. Next, the high-speed interfaces should be routed, and then slower interfaces. The following is the "ideal" signal routing priority used to lay out this board, with references to the corresponding schematic sheets, as appropriate.

1. Power supplies (sheets 13, 14)
2. Power/GND nets (including all bypass capacitors and wide trace power nets)
3. PLL loop filter and analog filter (sheets 4, 13)
4. Clock nets (sheets 4, 5, 9, 12)
5. SDRAM interface (sheets 4, 5)
6. PCI interface (sheets 4, 9, 10)
7. Ethernet interface (sheet 10)
8. Flash memory and serial EEPROM interfaces (sheets 4, 6)
9. IDE interface (sheets 4, 7)
10. ISA interface (sheets 4, 8)
11. Serial ports (sheets 4, 11)
12. Remaining signals

Clock Routing

The following considerations are important when routing clock signals.

Unmatched Length Clock Signals

The clock signals listed below should be routed without any length matching requirements. These traces should be as short and direct as possible between the source and destination pins. The trace width and spacing requirement (in 1/1000ths of an inch) is listed alongside the net name:

- X32kHzIN (5/15)
- X32kHzOUT (5/15)
- R33RPU (5/15)
- X33.333MHzOUT (5/15)
- X33.333MHzIN (5/15)
- CLK14MHz (5/15)
- CLK8MHz (5/15)
- SSI_CLK (5/10)

NOTE: The actual requirement is shown. Some traces on the board are wider than necessary because of component changes made in the design process.

Matched Length Clock Signals

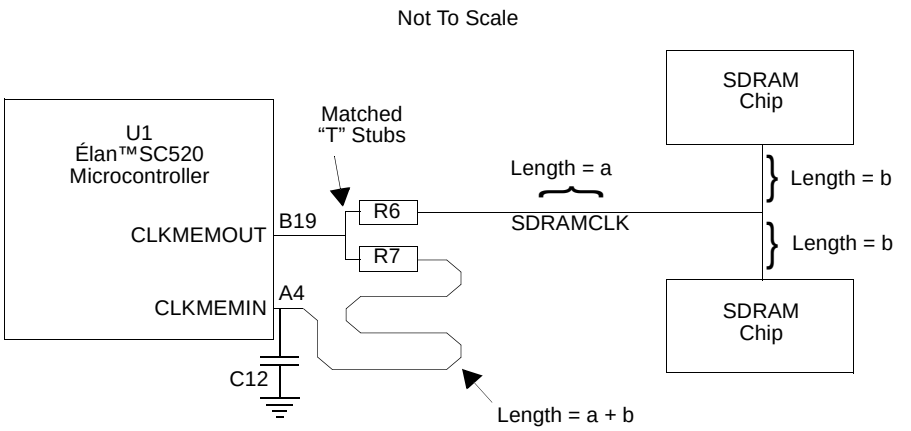
There are two clock signals that have length matching requirements: the SDRAM clock (66 MHz), and the PCI clock (33 MHz). For each of these clocks, the total trace length from the microcontroller output pin to each of the corresponding target pins must be matched. (There is no length matching requirement between the PCI Clock nets and the SDRAM clock nets.)

To equalize clock lengths, the board designer measures from the clock output pin of the microcontroller to the input pin of each target device. This includes the trace length to the series termination resistor, and from the series resistor to the input pin of the target device. The designer ignores the trace length from the target device input pin to the R-C or Thevenin termination (if any).

When equalizing clock trace lengths, the distance to the target pins must match to within a difference of 0.004 inch between the longest and shortest trace. In other words, there is a ±0.002-inch tolerance to the trace length from either of these clock outputs.

SDRAM Clock (66 MHz)

The CLKMEMOUT output on the ÉlanSC520 microcontroller is paired with the CLKMEMIN return input. As shown in Figure B-2, and on sheet 5 of the schematics, the goal in routing this clock signal is to make the traces the same length from CLKMEMOUT to each target device, and also the same length as the return signal trace to CLKMEMIN.



Notes:

Make the total trace length the same from the CLKMEMOUT pin to each SDRAM clock pin, and from the CLKMEMOUT pin to the CLKMEMIN pin.

Figure B-1. Memory Clock Routing

To do this, first the series terminator resistors on the CLKMEMOUT net (R6 and R7) are placed as close as possible to the microcontroller. A “T” routing pattern is used so that the trace length from the microcontroller output pin to either resistor is the same.

From series resistor R6, the SDRAMCLK net is routed to the SDRAM chips (U2 and U3), again using a “T” routing pattern so that the trace length to either SDRAM chip is the same. Then the actual trace length is measured from resistor R6 to each SDRAM chip (U2 and U3) and averaged, and the resulting value used to route a matched-length trace from series resistor R7 to the CLKMEMIN pin on the microcontroller.

To verify the lengths are matched, each trace length is measured from the CLKMEMOUT pin on the microcontroller to the appropriate series resistor, and then from the series resistor to each target pin. The longest and shortest trace lengths from the CLKMEMOUT pin to any target pin must be within 0.004-inches of each other.

The AC termination capacitor C12 (shown on schematic sheet 5) is placed as close as possible to the microcontroller, and as close as possible to where the CLKMEMIN trace is routed. The value of C12 is adjusted to fine-tune the clock timing. As shown in Figure B-2, increasing or reducing the value of C12 increases or reduces the rise time of the CLKMEMIN return signal, so it can be more closely aligned with the rising edge of the SDRAMCLK signal at the SDRAM chips.

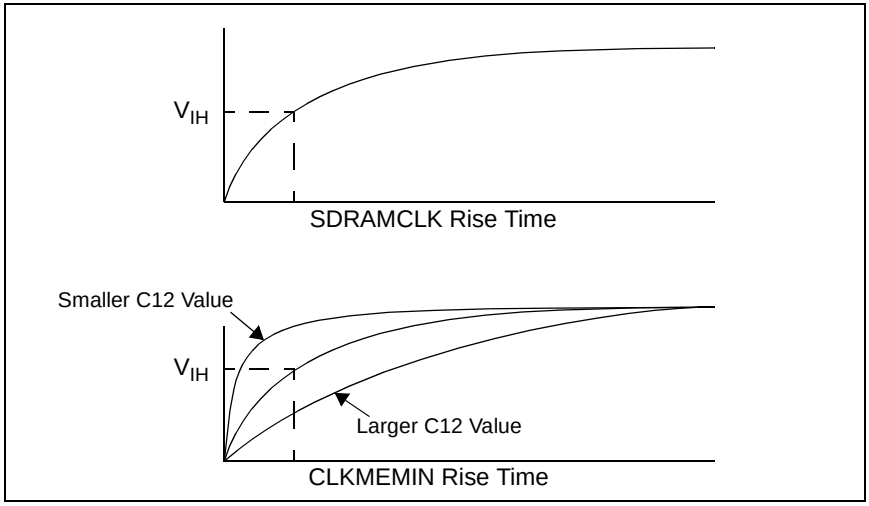


Figure B-2. Using C12 to Fine-Tune CLKMEMIN Timing

PCI Clock (33 MHz)

Similar to the SDRAM clock, the goal for the PCI clock routing is to make the PCI clock for the Ethernet chip, for each add-in module, and for the feedback path to the microcontroller, all the same trace length. However, the situation is more complicated because each successive add-in module adds 0.662 inches to the PC/104-Plus signals. Also, Modules 3 and 4 share the same clock net. To account for this, the clock trace to the PCI connector is shorter for each successive module, as shown in Figure B-3 on page B-7.

Thus, referring to the total trace length on the board, the clock traces are longest (both the same length) to the Ethernet chip and to the CLKPCIIN feedback pin on the microcontroller. The trace to the Module 0 clock pin on connector J4 is 0.662 inches shorter than the Ethernet (and feedback) clock traces, and the trace to the Module 1 clock pin on J4 is 0.662 inches shorter than the Module 0 clock trace.

Likewise, the traces to the J4 clock pins for Modules 2 and 3 are each 0.662 inches shorter than for the previous module. However, because Modules 2 and 3 share the same clock signal, the clock trace goes first to the Module 3 clock pin, and then a 0.662-inch long trace connects the Module 3 clock pin to the Module 2 clock pin.

Note that only the length of the trace from the output pin of the clock buffer to the target pin on the PCI device is important. The goal is to equalize the propagation time of the clock signal to all the attached PCI devices. The trace length to and from series termination resistors is considered. But the trace length to any pullup resistors, R-C termination, or Thevenin termination should be ignored.

In summary, the following formula expresses the trace length rules for the PCI clock signal. Refer to the signal names in Figure B-3 on page B-7.

CLKC1 + PCICLK0 (to Ethernet)

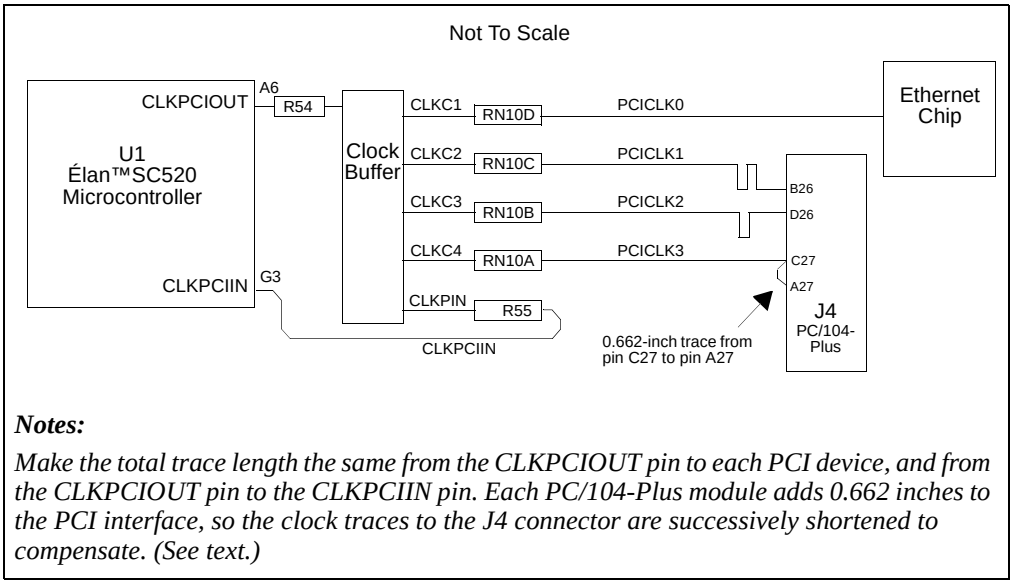
= CLCK2 + PCICLK1 (TO J4 PIN B26) + 0.662 INCH

= CLKC3 + PCICLK2 (TO J4 PIN D26) + (2 * 0.662 INCH)

= CLKC4 + PCICLK3 (TO J4 PIN A27) + (3 * 0.662 INCH)

= CLKC4 + PCICLK3 (TO J4 PIN C27) + (4 * 0.662 INCH)

= CLKPIN + CLKPCIIN



Notes:

Make the total trace length the same from the CLKPCIOUT pin to each PCI device, and from the CLKPCIOUT pin to the CLKPCIIN pin. Each PC/104-Plus module adds 0.662 inches to the PCI interface, so the clock traces to the J4 connector are successively shortened to compensate. (See text.)

Figure B-3. PCI Interface Clock Routing

Ethernet Section

The Ethernet section of the board (sheet 10 of the schematics) has some special layout considerations. These constraints concern the connections between the Ethernet chip (U8) and the RJ-45 connector (J5).

The RJ-45 connector, J5, is placed as close as possible to U8, the Ethernet controller chip, and U8 is oriented so that the pins that connect to J5 are as close to the connector as possible, so the nets connecting U8 to J5 can be as short and directly routed as possible.

Do not intermix any other nets within the U8 to J5 signals. This interface runs at 100 MHz, so it is important to keep other signals away from the interface signals. In particular, the U8 to J5 nets include two differential signal pairs, TX+, TX-, and RX+, RX-. The signals in each pair are routed 0.005 inches apart, and at least 0.015 inches from the other pair, or from any other signals.

The routing for TCTC and RCTC should also be short and direct, but they should not interfere with the differential pairs. Give priority to the routing of the TX+, TX-, RX+, RX- signals over all other signals connecting to the RJ-45 connector (J5).

Battery Power

The backup battery circuit needs some care during routing. It is important to route the entire backup battery circuit with wide traces and connect it back to the ÉlanSC520 microcontroller with wide traces. Wider traces have less resistance, so the voltage drop across the board will be minimized by using wide traces.

The backup battery circuit is shown on sheet 14 of the schematics. The following nets are in this circuit:

- MMBD-A
- VBAT
- MMBT-C
- MMBT-B2
- MMBT-B
- MMBT-C2
- BBATSEN
- VCC_RTC

Routed Power Nets: VCC12, VCC5M, VCC12M

VCC12 is brought onto the board through a 3-pin barrel connector in the power supply area. In this section of the board, VCC12 is a split plane on the VCC5 plane layer. Using a section of the VCC5 plane for a VCC12 plane allows the greatest current carrying capacity for the VCC12 net to feed the three switching power supplies. VCC12 also goes to the expansion connectors on the board. The VCC12 trace should be routed to the expansion connectors as a wide (0.35 inch or wider) trace on a signal layer.

VCC5M and VCC12M are the –5-V and –12-V power rails, respectively. Both of these voltages come from small banana jacks. Both of these nets go only to the expansion connectors. Both of these nets should be routed as wide (0.035 inch or wider) traces on a signal layer.

PLL Loop Filter/Analog Filter

There are two filter circuits required by the ÉlanSC520 microcontroller. The PLL loop filter circuit is shown on sheet 13 of the schematics. The analog filter is shown on sheet 4 of the schematics. Both of these filters need their components placed as close as possible to the microcontroller. Both of these circuits need the components routed together with wide etch.

Neither of these filter circuits should have other traces running through them. In other words, route these filters early in the design, do not route any other signals through their routing, and give these circuits priority over other routing.

For the PLL loop filter, the following components and net names are involved: TC9, R59, C137, C138, LP_PLL1, LP_RCS, VCC_ANLG, and VSS_ANLG

For the analog filter circuit, the following components and net names are involved: R2, C2, C3, TC1, GS1, VCC_ANLG, VSS_ANLG

Note that VCC_ANLG and VSS_ANLG are in both filter circuits.

VCC_ANLG is generated through R2 from the VCC_CPU net. R2 serves to filter out digital switching noise from VCC_CPU so it does not reach VCC_ANLG. The layout uses a wide (approximately 0.035-inch) trace to bring VCC_ANLG out of R2 and distribute it to the microcontroller and other components in these circuits. The layout double- or triple-routes the VCC_ANLG with traces as wide as possible to reach the appropriate ball inside the microcontroller's BGA footprint. Several parallel traces that are thin enough to enter the BGA footprint give a lot of current-carrying capacity with low resistance.

VSS_ANLG from all the components is routed together with wide traces into a single point, where it connects into the GND plane. A Ground Short (GS1) component is used to drive the netlist so that this single-point GND connection can be made properly. The GS1 component also allows the layout software's real-time error checking features to be used.

Interplane Capacitors

Depending on how the power planes are created and split, it is usually necessary to use some interplane capacitors in a design. These capacitors are used to tie two split planes together (like VCC3 and VCC5), and to give the high-frequency AC return currents a way to jump across the plane split, from one power plane to another.

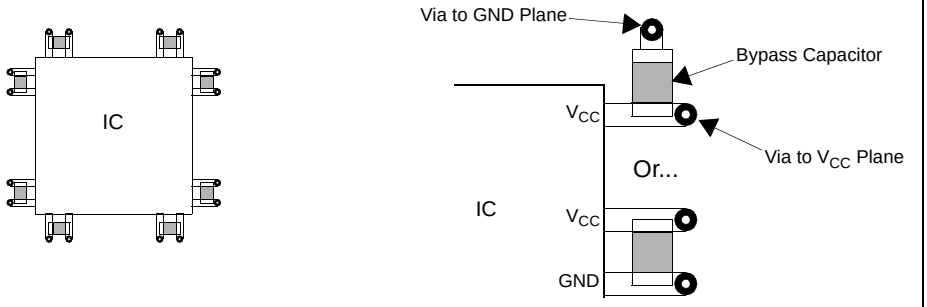
Interplane capacitors are placed amongst the signals where they cross a plane split. They are critical to include in the design for proper high-speed operation of the board. Until the board is completely routed, however, it is impossible to know exactly how many signals cross plane splits, and where the signals make the crossing. After the design is routed, these capacitors are placed among the signals where they cross the plane splits, and wired to the appropriate power planes. The interplane capacitor requirement for a design can only be determined after routing is complete. sheet 7 of the schematics shows the interplane capacitors used in this design.

Bypass Capacitor Placement and Routing

Figure B-4 shows the ideal placement and routing of bypass capacitors. The capacitor is placed as close as possible to the power pin of the chip, and connected to the chip with a trace as wide as the IC pin. The via to the power plane is on the opposite side of the capacitor from the IC. This allows the power via to feed the capacitor, and the capacitor to feed the power pin of the chip.

This is the ideal case, but it is not always possible to make all bypass capacitor placement and routing look exactly like this, and trade-offs can be made. The most important features to remember are to use short, wide routes from the capacitor to the IC pin, and to place the capacitor between the IC and the power via.

For QFP and other chips with multiple power and ground connections, both sides of the capacitor can be tied to the IC, with one side tied to a VCC pin and the other to a GND pin. For a QFP package, try to have at least one bypass capacitor per side of the chip, and two if at all possible.



Notes:

For a QFP package, try to have at least one capacitor per side of the chip, two if at all possible.

Place bypass capacitors close to power pin of IC.

Use traces as wide as the IC pin. The via to the power or ground plane is on the opposite side of the capacitor pad from the IC pin.

Figure B-4. Bypass Capacitor Placement and Routing

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